STEREO CASSETTE DECK

TC-K60

US Model
Canadian Model
AEP Model
E Model
UK Model

SUPPLEMENT

File this supplement with the service manual.

No. 1
Feburuary, 1979

Subject: Circuit Operation

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SONY®
SERVICE MANUAL

SUPPLEMENT NO. 1

1. BSL (Brush and Slotless) Motor

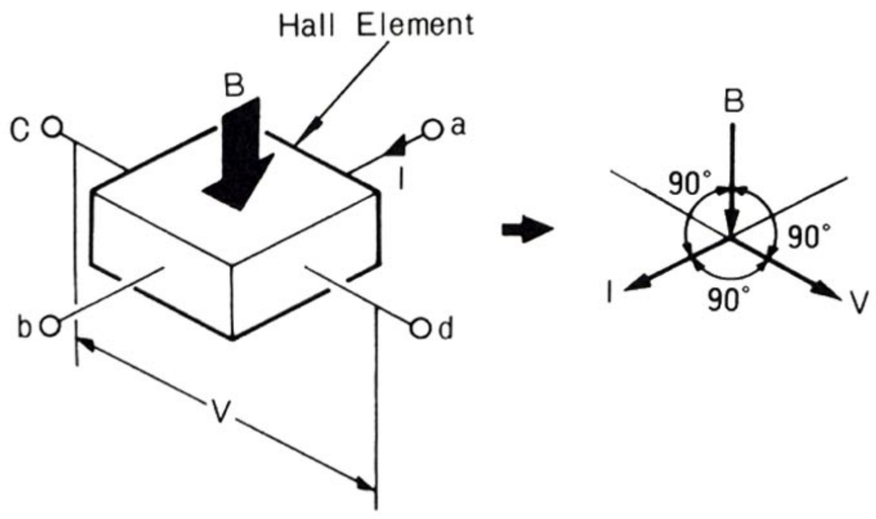
The BSL motor, which employs the hall element as an electronic switcher, has the low noise and the stable performance.

1) Hall Element

The magnetic field strength is converted into electrical signals by employing the Hall Effect.

Hall Effect:

When a metal strip is placed with its plane perpendicular to a magnetic field and an electric current flows longitudinally through the strip, a potential difference is developed across the strip at right angles to the current flow and to the magnetic field. The potential is proportional to amounts of the current and a strength of the magnetic field.



When the current I flows through the hall element (a—b), the potential **V** is developed across c—d.

Fig. 1

2) BSL Motor and Its Drive Circuit

The motor magnet is magnetized in 8 poles (sinusoidal patterns).

The constant current I is supplied to the hall element H1.

When the H1 comes to the N pole of the magnet, the voltage is generated in the H1.

This voltage is fed to IC1002-1 and Q1002 turns on.

Therefore, the current $\phi 1$ is supplied to the motor coils through Q1002.

At this moment, by the Fleming's left-hand rule, the magnetic force (F) is produced in the motor coils.

And the magnet rotates in the opposite direction of the magnetic force, since the motor coils are fixed.

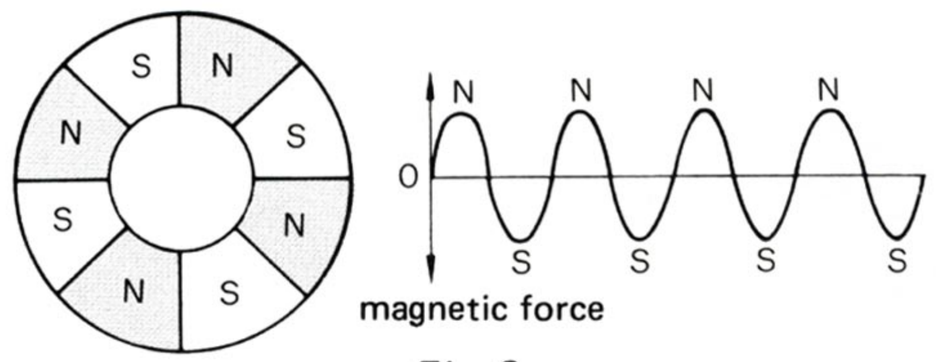


Fig. 2

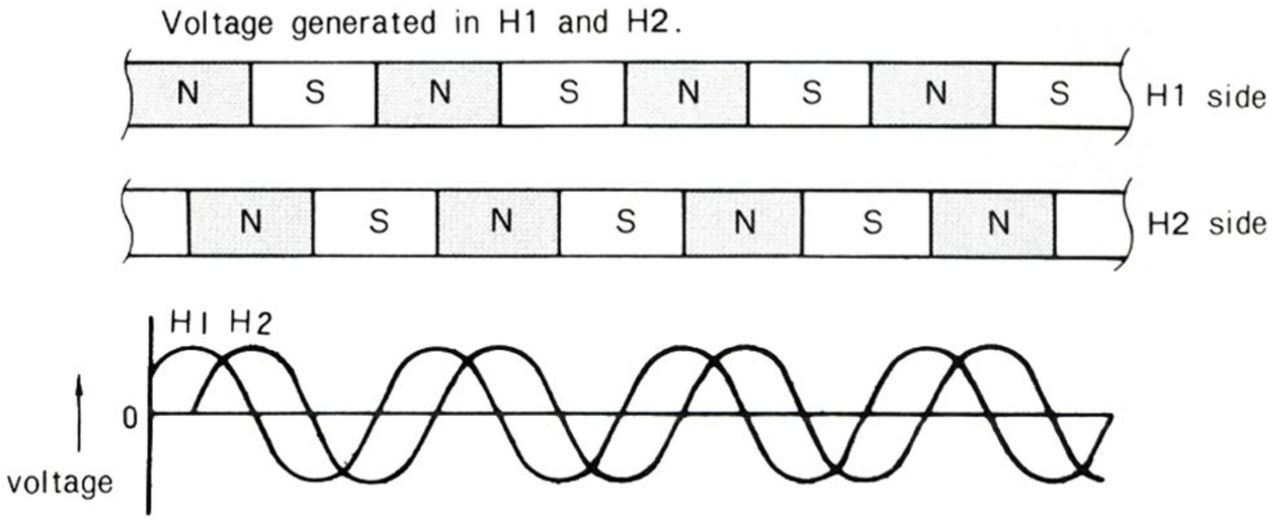


Fig. 3

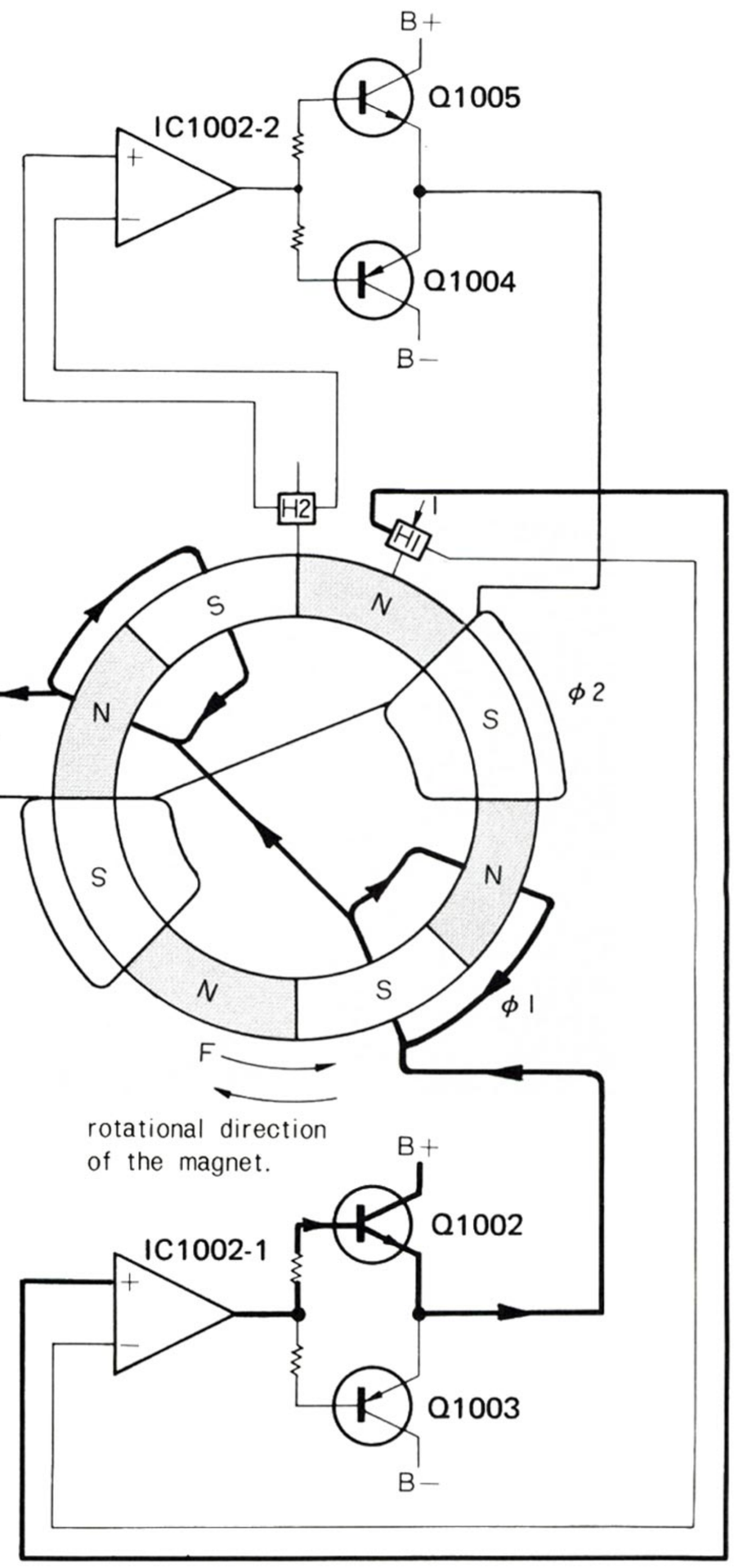


Fig. 4

2. AMS (Automatic Music Sensor) Circuit

This set is capable of automatic selection of up to 9 separate programs, this being achieved by detecting the interval between programs.

1) Automatic Selection Circuit (See Fig. 5.)

a) When S7 (MEMORY/AMS) is switched to the AMS position, a voltage is applied to terminal 5 (RBI) of IC601, resulting in [7] lighting up in D606 (Route ①).

b) When S17 (PROGRAM) is pressed, a program selection signal is applied to terminal 1 (UP INPUT) of IC601, and the selected program number is displayed in D606 (Route ②).

c) The FORWARD button is then pressed together with either the FAST FORWARD or REWIND button. When S15 (FAST FORWARD/REWIND) is switched on, a voltage is applied to the base of Q605, thereby turning the transistor on (Route ③). Terminal 4 (UP/DOWN) of IC601 will thus be switched to LOW level, resulting in the activation of the addition/subtraction circuit in this IC (Route ④). Furthermore, Q605 will also turn Q601 off, thereby cancelling the muting of the AMS detector input (Route ⑤).

d) The tape deck will now be in fast forward-playback or rewind-playback mode. Since S15 (FAST FORWARD/REWIND) is on, Q105 will also be on because of the voltage applied to its base. The high speed "gabble" during fast forward-playback or rewind-playback mode will thus be muted (Route ⑥).

e) The playback signal is amplified by Q602, 603, and applied to the base of Q604. When the tape reaches a blank section between programs, one pulse signal is applied to the base of Q604, thereby turning the transistor on. A subtraction signal is thus applied to terminal 2 (DOWN INPUT) of IC601 via C605 and R612, 613 to reduce (count down) the selected program number by one (Routes ⑦ and ⑧).

f) The selected program number is thus reduced until [0] is displayed in D606. Terminal 6 (PM OUT) of IC601 is then switched to HIGH level, resulting in Q609 and 611 turning on and activating the solenoid. The FAST FORWARD or REWIND button will then be released, putting the deck directly into playback mode (Route ⑨).

g) The solenoid is released again by applying a signal from terminal 3 (DOWN OUTPUT) of IC601 to the base of Q607 via the differential circuit formed by C612 and R636. Q607 thus turns off, and Q608 turns on, resulting in the muting of the Q609 base potential (Route ⑩).

2) D606 (LED) Muting When Power Switch Turned Off (See Fig. 5.)

When the power switch is turned off, the base potential of Q509 drops almost to zero very rapidly, resulting in the transistor turning off. Q606 consequently turns on, and terminal 5 (RBI) of IC601 is switched to LOW level. The D606 display will then promptly disappear (Routes ⑪ and ⑫).

3) Memory Stop Operation (See Fig. 5.)

a) Set S7 (MEMORY/AMS) to the MEMORY position.

b) When the REWIND button is pressed, S15 (FAST FORWARD/REWIND) and S13 (REWIND) will be both on, resulting in a high potential at the D603 anode (Route ⑬).

c) When the tape counter reaches 999, S12 (COUNTER) switches on. And while C613 is being charged up, a voltage will be applied to the base of Q610 turning the transistor on (Route ⑭).

d) Q610 also turns Q611 on, resulting in the solenoid being activated for "memory stop operation" (Route ⑮).

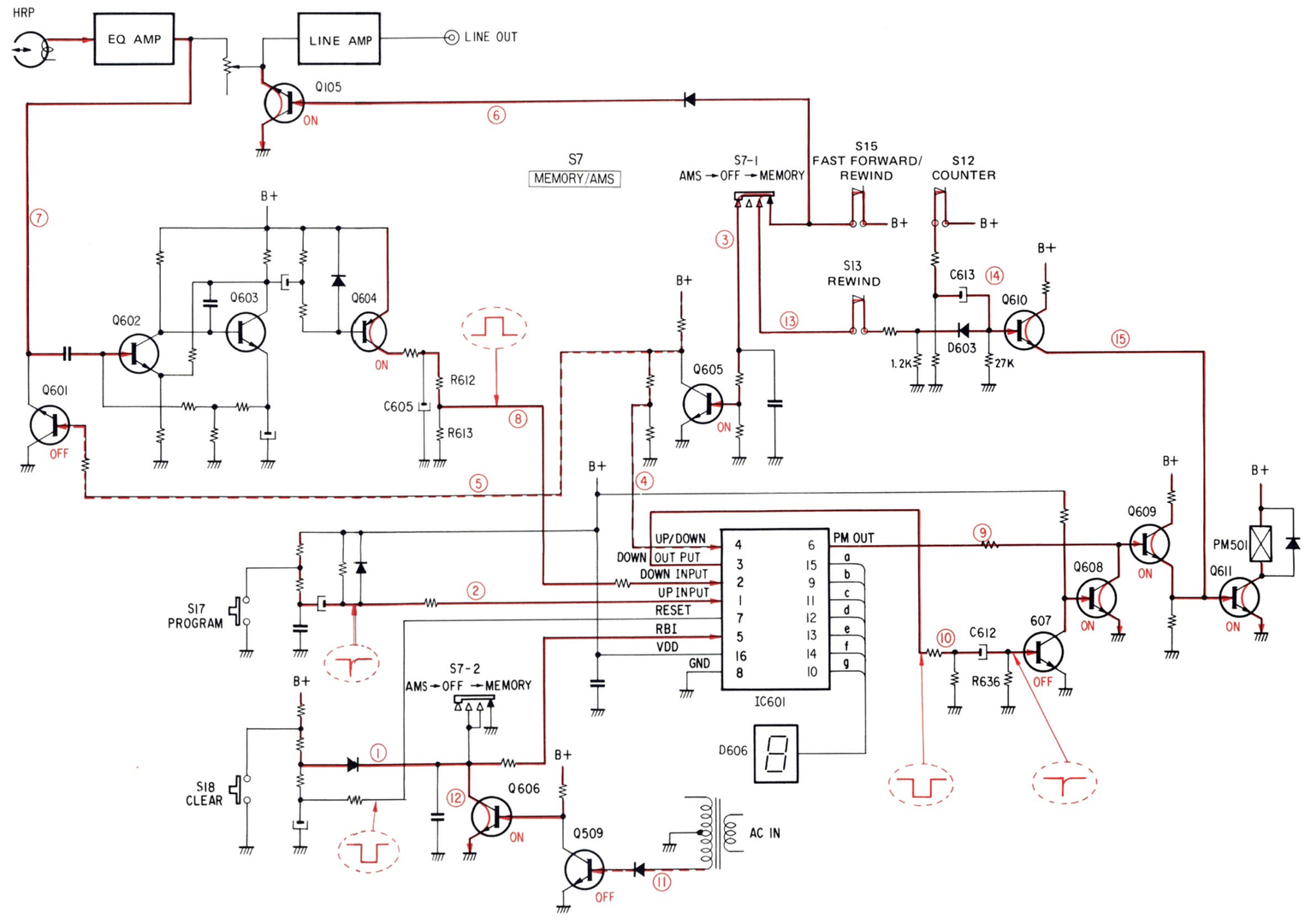


Fig. 5

MEMO

3. Liquid Crystal Peak Program Meter Circuit

This set also features liquid crystal peak program meters which display the playback and recording signals in analog bar graphs employing liquid crystal. These meters are also designed to memorize, and hold the peak levels.

1) IC901 (Liquid Crystal Peak Program Meter Control IC) (See Figs. 6 and 7.)

The 24-pin CMOS LSI, IC901, generates all the necessary signals required to drive the liquid crystal peak program meters.

a) Basic frequency signal
The basic frequency signal Ⓐ is generated by an oscillator in IC901, the frequency being determined by C904 and R909 connected to the C1 and R1 terminals of this IC.

b) Frequency division
The basic frequency signal Ⓐ undergoes 1/512 frequency division in the 9-bit synchronous up-counter (Ⓑ – Ⓙ).

c) Clock pulse Ⓛ
Playback and recording signals are converted into pulse signals when passed through the A/D converter. The clock pulse Ⓛ which serves as the reference pulse for this conversion is formed by passing waveforms Ⓚ, Ⓒ and Ⓓ through an AND gate.

d) Strobe pulse Ⓜ
This is reset signal for IC701 and IC751.
To obtain this signal, the BS terminal input and waveform Ⓙ are passed through an OR gate and then the OR gate output and waveforms Ⓑ – Ⓘ are passed through an AND gate.

e) Drive pulse
The liquid-crystal-drive pulse signal is produced as the Ⓘ output when the IC901 BS terminal input is HIGH, and Ⓙ when the input is LOW.

f) Auto reset pulse oscillation
An auto reset pulse signal is generated in the IC901 oscillator circuit and appears at the AROI terminal (Ⓝ). The frequency of the pulse is controlled by C903 and R908 connected to the C2 and R2 terminals of IC901.

g) Operation when S20 (AUTO RESET) is on
When S20 is switched on, the AUTO RESET terminal is set to LOW level (Ⓞ). Consequently, the auto reset signal appears as an inverted output (Ⓠ) at the PHR terminal.

h) Operation when S19 (MANUAL RESET) is on
When S19 is turned on, the MANUAL RESET terminal is set to LOW level (Ⓟ). The PHR terminal consequently remains at HIGH level (Ⓠ).

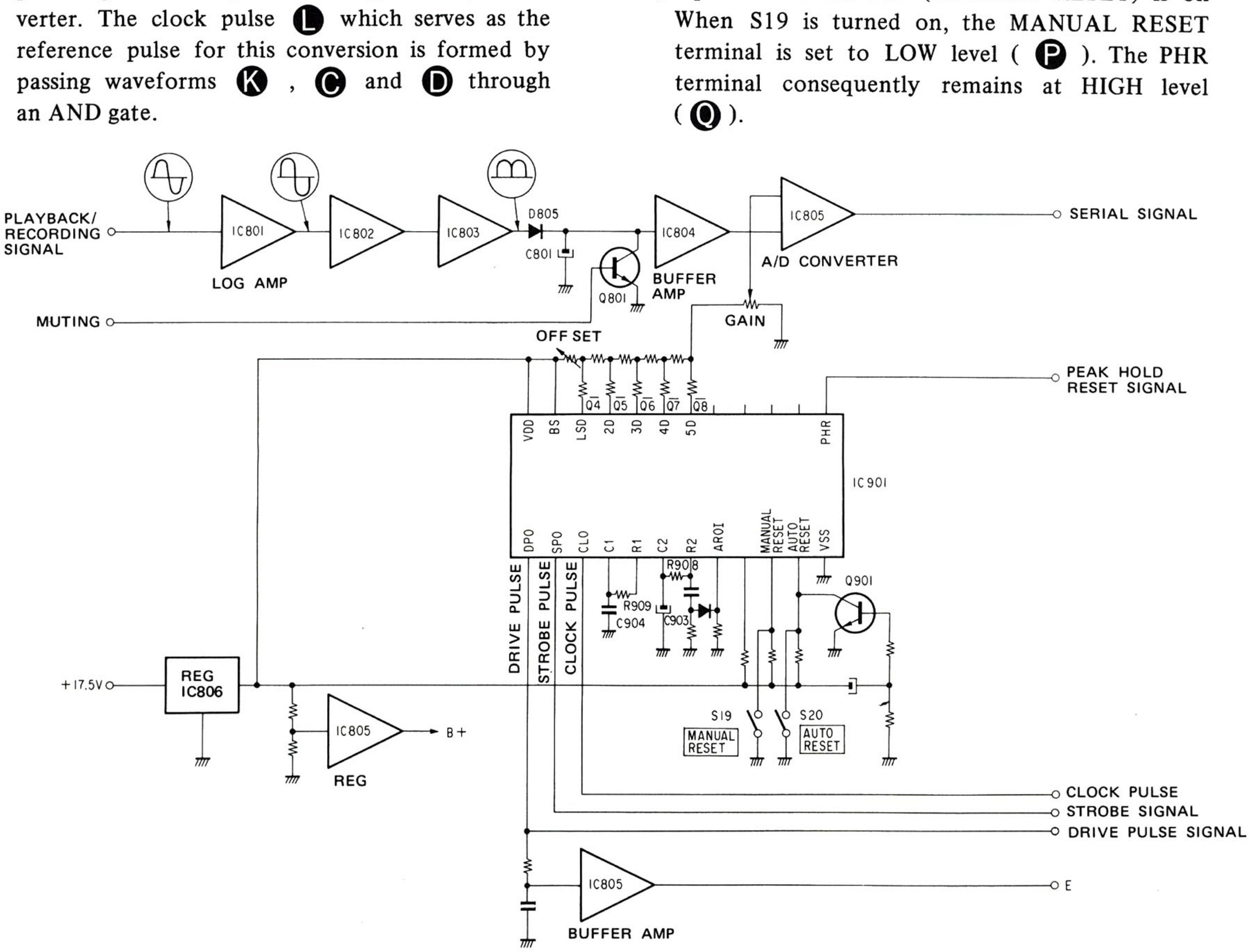


Fig. 6

2) A/D Converter (Serial Signal Generator Circuit) (See Figs. 6 to 8.)

The playback and recording signals undergo logarithmic compression in IC801 to provide a wider range on the meter scale. Then, to be able to detect both negative and positive peaks, the playback and recording signals are fully rectified by IC802, 803 and smoothed by C801. These DC signals are then applied to IC805 (A/D converter) via IC804.

Ⓡ-a, b, c indicates level variations in the playback and recording signals. The IC901 LSD, 2D, 3D, 4D, 5D outputs Ⓔ to Ⓘ form a comparator sawtooth wave Ⓢ after passing through the inverter and being added together. This signal is then applied to the IC805 A/D converter, resulting in playback and recording signal level variations expressed by the number of pulse signals appearing at the IC805 output (Serial signal Ⓣ).

Furthermore, to prevent meter indication drift at very low signal levels, the minimum level of the comparator sawtooth signal is adjusted to a level below 0V, thereby ensuring that the serial signal contains at least 1 pulse at all times. The minimum level in the liquid crystal meter will then remain on continuously.

3) Peak Hold and Peak Reset Circuit (See Figs. 9 and 10.)

IC701 and 751, 48-pin CMOS LSIs, are employed in the control of the liquid crystal drive, and peak level holding and resetting operations.

a) When S19 (MANUAL RESET) is on
When the serial signal Ⓣ is applied to the IC701 serial input by the IC805 A/D converter, a peak level signal derived from the serial signal will appear at the IC701 peak output. The serial signal and the peak level signal are then combined by OR operation in IC701, and both are displayed simultaneously in the liquid crystal meter.

b) When S20 (AUTO RESET) is on
Again the serial signal and the peak level signal are displayed simultaneously in the liquid crystal meter as described above. In this case, however, the peak level signal Ⓤ is reset within a 0.5 sec. interval (approx.) by the auto reset signal Ⓦ from the IC901 PHR terminal.

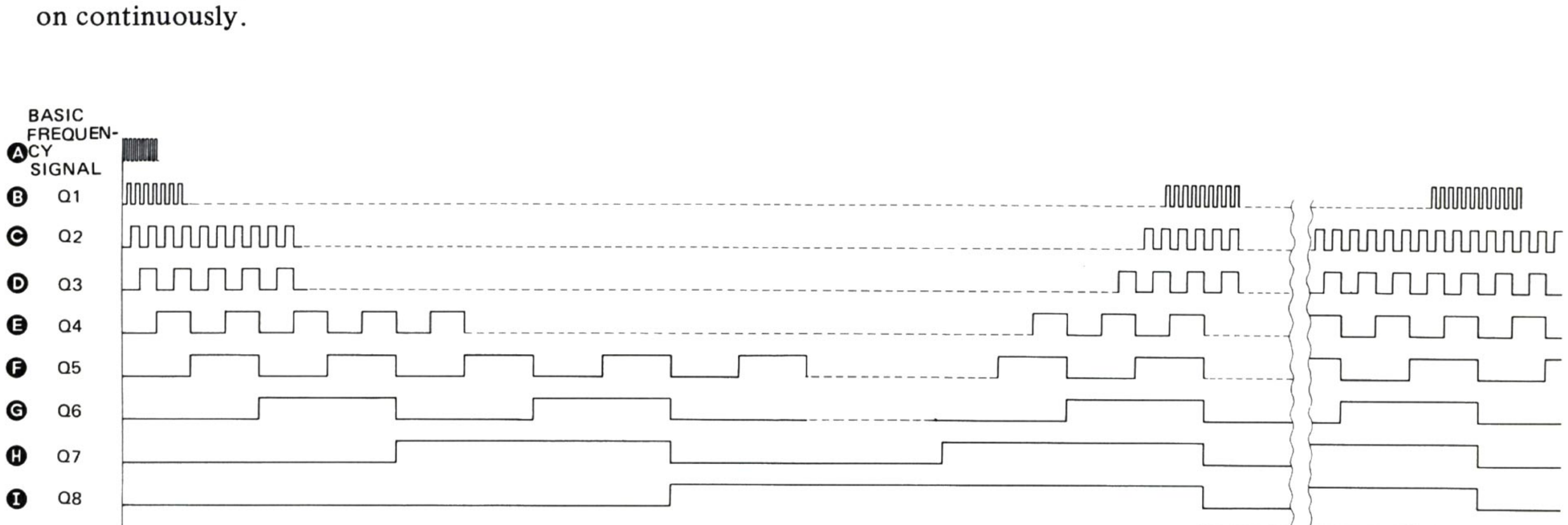


Fig. 7

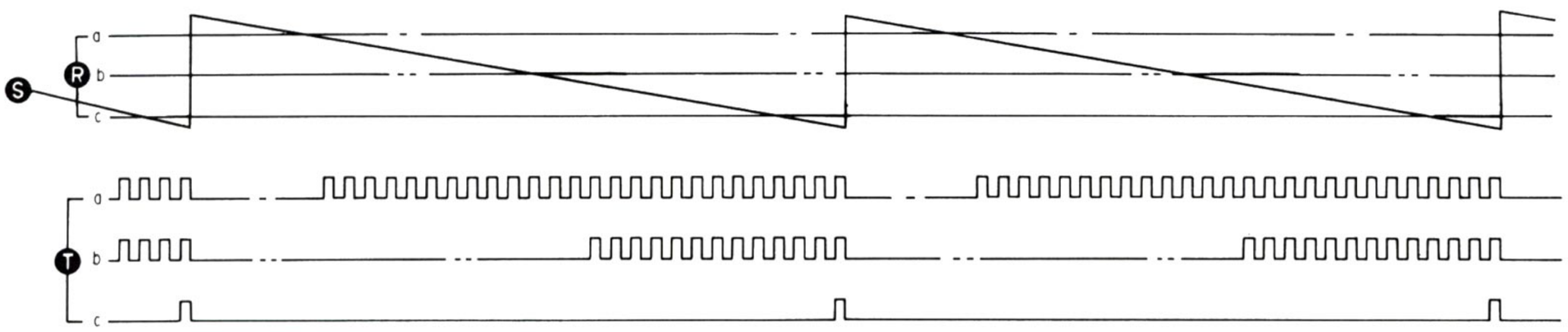


Fig. 8

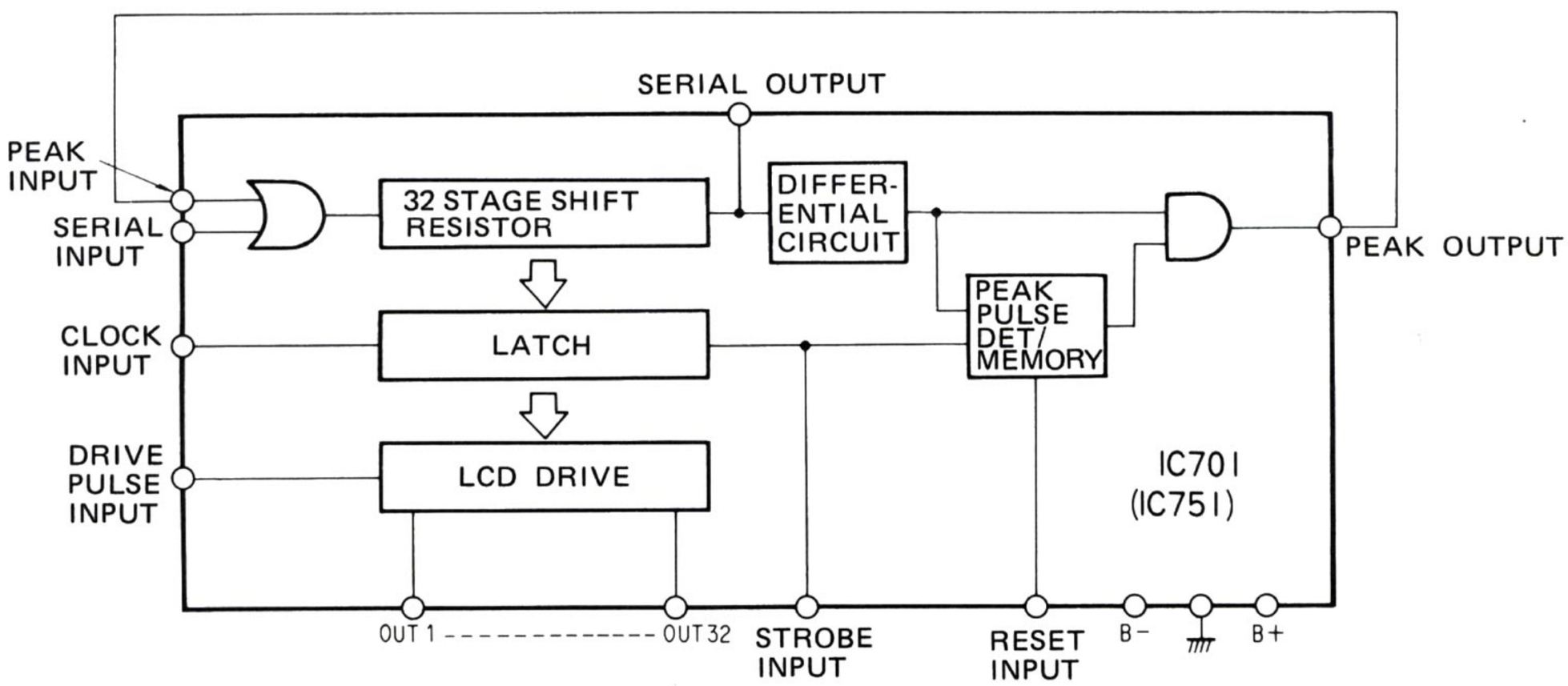


Fig. 9

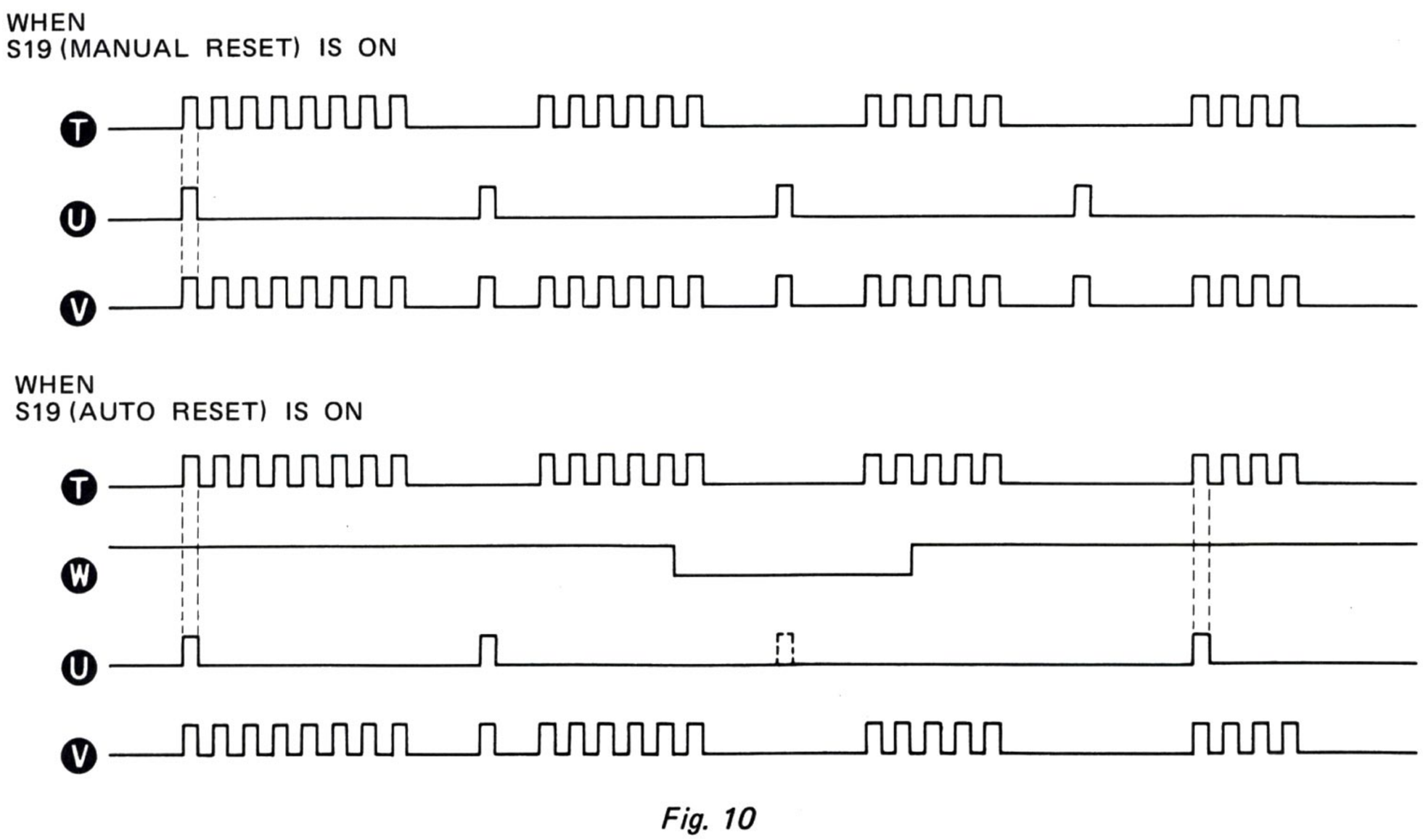


Fig. 10

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