FM STEREO TUNER

ST-J60/J60A

ST-J60:

US Model
Canadian Model
AEP Model
UK Model

ST-J60A:

AEP Model
UK Model

SUPPLEMENT

File this supplement with the service manual.

No. 1
October, 1979

CIRCUIT DESCRIPTION

FUNCTIONS ON THE PANEL

Indications

Frequency Indication (frequency coverage):

FM: US, Canadian model:
87.50 MHz – 107.9 MHz
(in 200 kHz step)
AEP, UK model:
87.50 MHz – 108.00 MHz
(in 50 kHz step)

MEMORY Indication:

When the MEMORY switch is pushed, MEMORY is displayed in the display tube for about 3.5 seconds and it shows that the memory writing is ready.

Preset Station Indication:

When one of the eight preset switches is pushed and the proper memory is called up, or a station is preset by one of eight preset switches, an appropriate window shows up the station name or number by lighting up.

AUTO DIMMER Indication:

This device receives surrounding light and changes intensity of the display tube's display in two steps according to the strength of the lihgt.

Switches

MEMORY Switch:

When the MEMORY switch is pushed, "MEMORY" is displayed in the display tube and it shows that the memory writing is ready. The period that can be used for memory writing is about 3.5 seconds. After about 3.5 seconds, "MEMORY" display disappears automatically. When one of the eight preset switches is pushed in about 3.5 seconds, the receiving frequency is memorized in the appropriate memory location and "MEMORY" display disappears. Push the MEMORY switch once again when it is needed to cancel this function after the MEMORY switch is pushed.

AUTO TUNING Switches (<, >):

The switch marked with > works for scanning up the receiving frequency and that marked with < works for the scanning down the receiving frequency, and the scanning automatically stops on receipt of the stop signal. When this switch is kept depressed, the scanning up or down operation continues until a stop signal is received by the scanning circuit.

SONY®
SERVICE MANUAL

On receipt of the stop signal, the scanning operation stops once for about 0.4 second and starts scanning again. When the scanning has reached to the lowest frequency, i.e., 87.50 MHz, the scanning now jumps automatically to the highest receiving frequency, i.e., 107.90 MHz or 108.00 MHz, and vice versa. Thus the scanning continues until a station is received again.

MANUAL TUNING Switches (<, >):

When one of these two switches for tuning up (>) and tuning down (<) is pushed once, the tuning frequency moves up or down in one tuning step, i.e., 200 kHz or 50 kHz. When this switch is kept depressed, the tuning now becomes in a scanning mode with a slower speed than that in the AUTO TUNING mode. In the latter case, the stopping of the frequency scanning like in the AUTO TUNING mode is not made.

Preset Switches (eight):

By using the non-volatile memory IC CX761, station memory is possible up to eight stations. In the condition ready to writing a data in the memory IC with the MEMORY switch pushed, and then an appropriate preset switch is pushed, a station or frequency is written in the corresponding memory location. These switches are also used for calling up the stations or frequencies already preset.

MEMORY SCAN Switch:

When the MEMORY SCAN switch is pushed, an automatic scanning starts to scan the memorized stations in about 3.5 second increment. When a desired station is received, the receiving condition is made by pushing the appropriate preset switch and the scanning stops at this station. This automatic scanning also stops when a preset switch is pushed at random base.

STEREO MUTING Switch:

When this switch is turned ON, a comfortable station selection is made without being bothered by the noise usually encountered between two strong stations, and any weak stations are skipped. The FM stereo programs are received in the stereo mode with the switch turned ON. When this switch is turned OFF, the muting effect is also turned off and the FM stereo programs are received in the monaural mode.

SIGNAL MULTIPATH Switch:

When this switch is set to SIGNAL position, the signal strength of a station being received is indicated in the SIGNAL indicator (1–5). When this switch is set to MULTIPATH position, the degree of the multipath is indicated in the MULTIPATH indicator (1–5).

CAL TONE Switch:

When this switch is turned ON, a 400 Hz signal of a level equivalent to 50 % (–6 dB) modulation is put out from the OUTPUT jacks.

On the Memory:

Last-station memory:

The frequency of a station being received just until turning off the POWER switch is automatically memorized in the memory and this station, i.e., the last station is recalled or reread when the POWER switch is turned ON again. When the memorizing station is changed, the new station is automatically memorized in the memory IC after four seconds of the station changing.

CONFIGURATION

This set is a crystal-controlled digital PLL synthesized tuner. Fig. 1 shows the portion of the front end, synthesizer, PLL and their associated circuits. The oscillation frequency from the VCO (Voltage-Controlled Oscillator) is divided by 20 in the prescaler. The output frequency from the prescaler is routed to the programmable divider and is further divided by a factor P. In Fig. 1, P = 1007. The receiving frequency is decided by the value of P which is changed by the controller located outside of the PLL synthesizer. The output signal from the programmable divider is now routed to the phase comparator. To this phase comparator, a signal (fixed 5 kHz) from the frequency divider which divides the output frequency of the reference crystal oscillator is also applied. Thus the local oscillator's and crystal oscillator's frequencies are phase-compared in the phase comparator, and a control signal is put out. The output signal from the phase comparator goes to the low-pass filter and a smoothed DC control voltage is obtained. This DC control signal is now applied to the varicaps in the local oscillator and radio-frequency amplifier stages.

In this set, a microcomputer is used in the place of the controller. This microcomputer also controls the whole system of the set, i.e.,

a. monitoring of function switches by scanning
b. writing of received frequency and/or reading of memorized frequency
c. generation of muting signal
d. dimmer control

etc.,

PLL SYNTHESIZER (Refer to Fig. 1)

1) The reference crystall oscillator generates a 5.76 MHz signal. This signal is then divided by 1152 in the frequency divider and a 5 kHz signal is obtained. This 5 kHz signal is applied to the phase comparator. Ths phase comparator generates a control signal by comparing the phases of the above mentioned 5 kHz signal and that coming from the programmable divider. The control signal is applied through the low-pass filter to the varicaps in the local oscillator, and the oscillation frequency is corrected. This circuit operation continues until the frequencies and phases of the two input signals into the phase comparator become in the equal values.
2) The local oscillator's frequency is decided by the division ratio of the programmable divider, that is, the instruction from the controller.
3) When the instruction from the controller is "Divide the frequency by 1007", the local oscillator's frequency is

$$\frac{1}{\frac{1}{20}} \times \frac{1}{\frac{1}{1007}} \times 5\ (\text{kHz}) = 100.7\ \text{MHz}$$

where,

1/20 means the division ratio of the prescaler

1/1007 means the division ratio of the programmable divider.

5 means the resultant output frequency 5 kHz from the programmable divider.

So, the receiving frequency becomes in 90.0 MHz by subtracting the intermediate frequency 10.7 MHz from 100.7 MHz.

4) Thus the all that is needed for selecting a station is only the instruction to be applied to the programmable divider when the local oscillator is composed of the PLL as outlined above. The instruction of the division ratio to the programmable divider is, in fact, very complexed and critical. So, this instruction is made by utilizing a microcomputer which contains a nonvolatile program made exclusively for this set.

MICROCOMPUTER μPD552C014 (IC606)

The microcomputer acts as the central control and controles the whole system of the set. It receives information from the function switches on the front panel, puts out the station-selecting data to the programmable divider, and also puts out instructions to the display and audio amplifier sections. It also works for the writing of the received frequencies, and reading out the memorized frequencies.

A simple explanation of the microcomputer operation follows:

1) Microcomputer

The microcomputer, literally, means a microscopic electronic computer. However, a computer, being more than a calculator, has functions similar to those of the human brain.

The human brain has three major functions.

1) Storage; a capacity to store (memorize) previously received information.
2) Decision; the ability to compare information obtained from the sense functions (eye, hand, leg, etc.) with the memorized information and to put out the most suitable instruction.
3) Instruction processing; the ability to transmit the decisions to the body (hand, leg, etc.) and make it operate in the required way.

In the computer, the decision making, processing, and instruction generation part is called the CPU (Central Processing Unit): the storage part is the ROM (Read Only Memory = memory for only reading) or RAM (Random Access Memory = read/write portion): and the body corresponds to the I/O (I/O Interface = input/output devices).

To give a comprehensive name to all these electric circuits and functions, we use the term "computer".

There are however the following differences between the human brain and a computer.

(1) In the computer storage, matters once memorized will not be forgotten.
(2) The computer cannot make decisions regarding any non-stored information.
(3) In speed of processing or decision making, a computer is much faster.
(4) The computer cannot store as much as the human brain.

1) CPU

The CPU is the most important part of a computer and assumes a central role. Considering the CPU as a digital circuit, by applying a signal "we want to read contents of an address" at the input, the requested contents are output in response to the instruction. In other words the CPU carries out the processing taking out a sequential processing program from the program into which the instructions were entered and decoding the instructions.

In this device, a 4-bit CPU is employed. The 4-bit CPU is more suitable for system control rather than that for computations.

The CPU configuration in this device consists of a PC (Program Counter), STACK, DP (Data Point), ACC (Accumulator), ALU (Arithmetic Logic Unit). Each of these will be described below.

(a) PC (Program Counter)
This is a register which stores the address of the contents of the ROM to be processed next, so that the execution sequence of the program will be correctly followed.
Each time after executing one instruction, this is increased by + 1.

(b) STACK
This is a register for storing aside the contents of the PC when a subroutine is called or during interrupts.

(c) DP (Data Point)
This is a register which specifies the address of RAM.

(d) ACC (Accumulator)
This is a register for storage of the operation results of ALU or as a temporary storage external to the CPU.

(e) ALU (Arithmetic Logic Unit)
This is the arithmetic logic operation unit, which has functions of binary addition, increment, decrement, exclusive OR, comparison, etc.

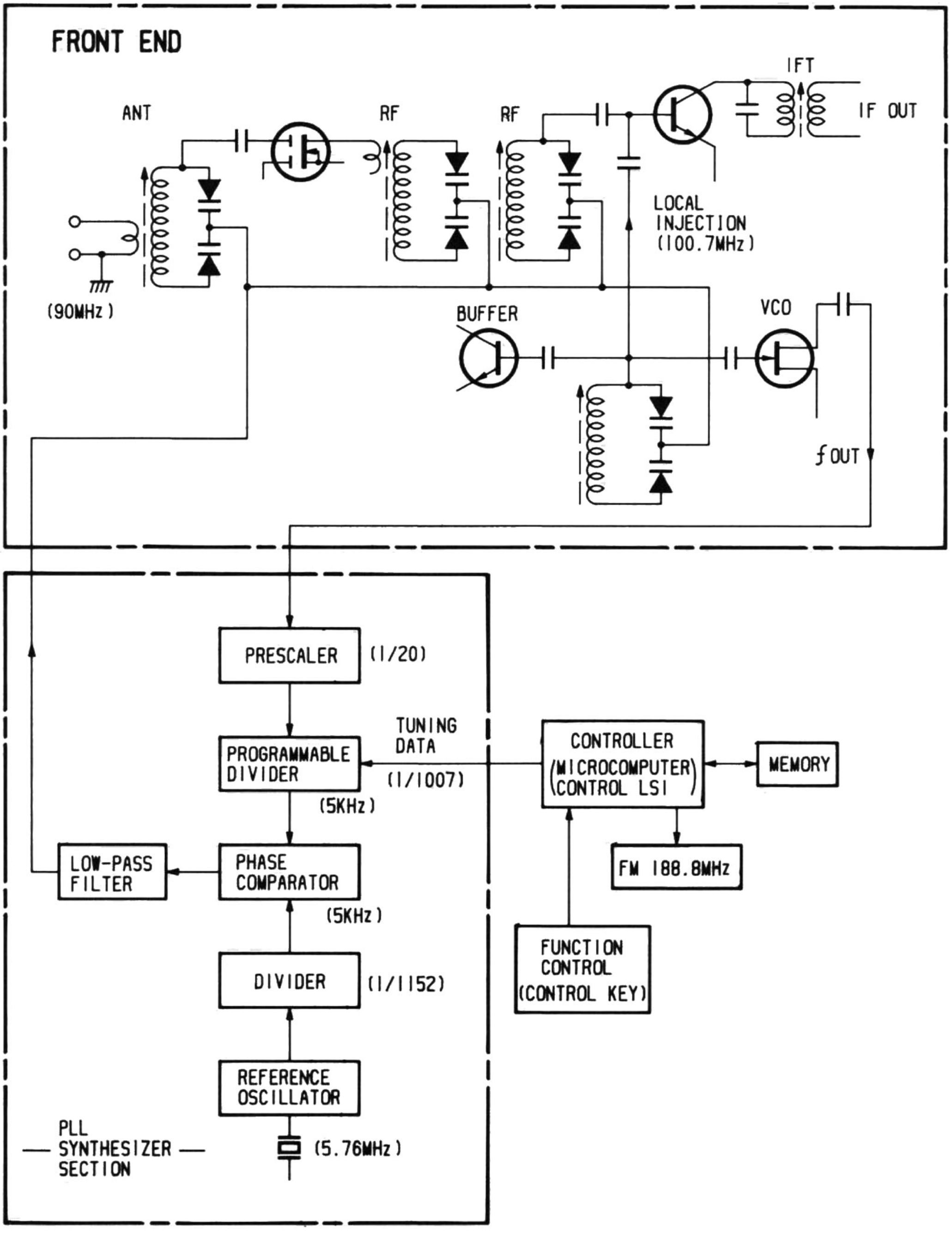


Fig. 1

2) Memory (Storage device)

(a) ROM (Read Only Memory)

This memory is only for reading. The following are the features of ROM. (1) It is difficult to modify the stored contents because it is impossible to rewrite the contents of ROM by a program. (2) Even if the power source is cut off, the contents stored in a ROM will not be erased. Utilizing these features, the ROM stores the data which should not change. Further, when no data is needed, the power dissipation can be made lower by switching off the power source.

In this device a 1000 word x 8-bit mask ROM is employed for storing the program, etc., and is addressed by the PC.

The features of a mask ROM.

(1) The chip size is smaller than that of a ROM.
(2) It is suitable for storing considerable data of the same pattern.
(3) It can be cheaper than a P-ROM in mass manufacture.

(b) RAM (Random Access Memory)

This is a memory in which data can be recorded or can be read out at any position in any sequence by specifying the address and the bit. In this microcomputer, data is stored in a 64 x 4-bit static RAM and is addressed by DP (Data Point).

The features of the static RAM.

(1) The power dissipation per bit is high.
(2) Operation speed is slow.
(3) Because data does not get erased with time, refreshing is not needed.

2) Programming

A program is a description of the sequence of operations to be followed by the computer expressed in a language that the computer can comprehend, and which is based on the basic functions possessed by the computer.

The language which the computer can understand is called the "machine language". The machine language descriptions are those that the computer can decode immediately and execute, and are expressed

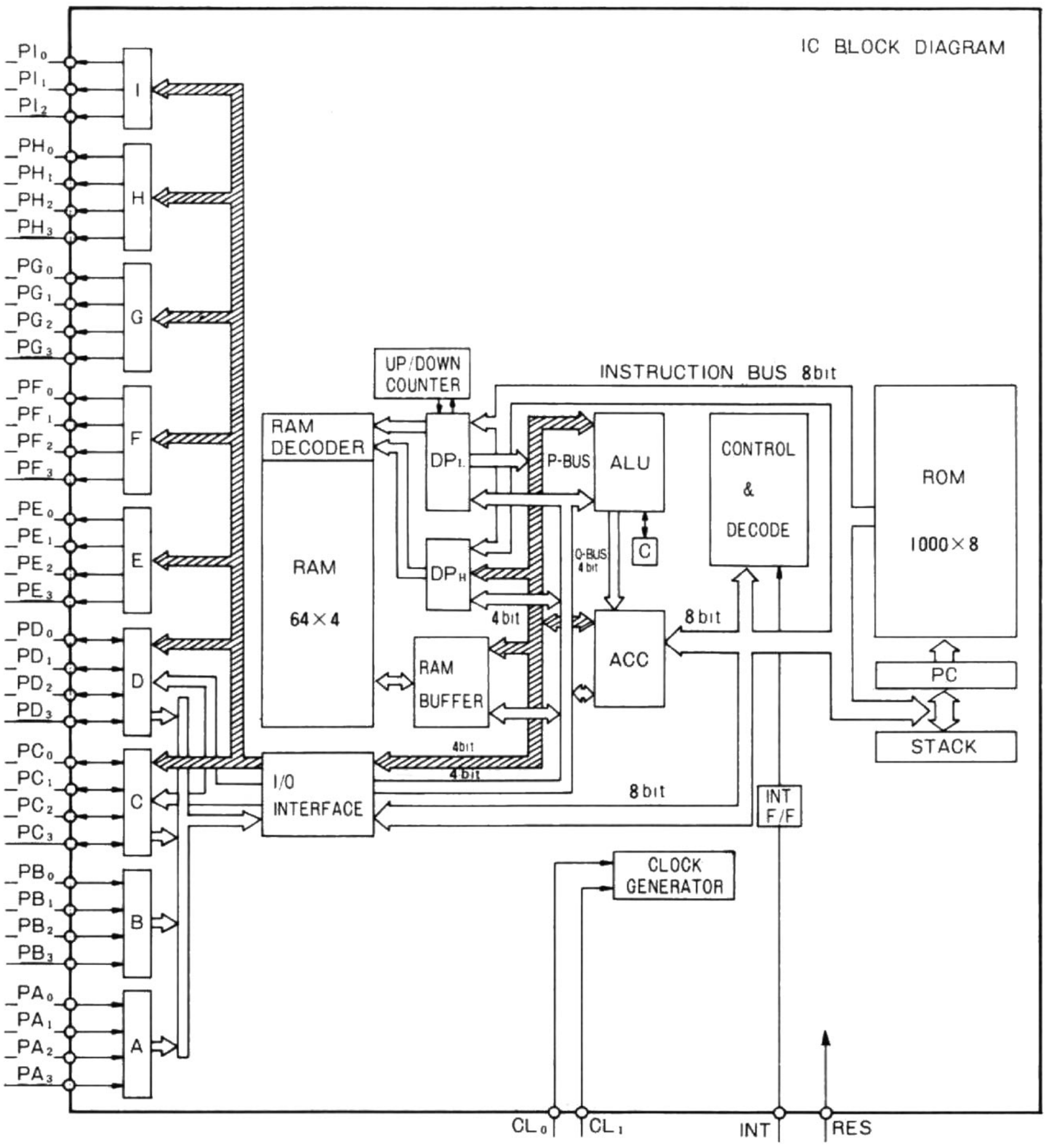


Fig. 2

with the combination of "0" and "1". However, the machine language can be different for different computers.

Because the machine language is very much different from the English language, it is translated into an assembler language, and is expressed with mnemonics (these express instruction words, with letters which function as a mnemonic aid).

Some examples of descriptions in the machine language and in the assembler language employed in this microcomputer are given below.

Outline of μPD552C014:

This is a four-bit control microcomputer composed of ALU, ROM, RAM, I/O Ports and control circuit all of which are processed in four-bit parallel manner and are included on a small single chip.

P-channel MOS
ROM (100 x 8-bits)
RAM (64 x 4-bits)

Input Ports A and B
Input/output Ports C and D
Output Ports E, F, G, H, and I
} four-bits each except for Port I which is three bits

Clock Frequency: 360 kHz

Input signal is obtained from terminal 4 of the divider output in PLL μPD2819C.

42-pin Plastic Dual-in-Line Package

I/C Ports:

Table 1

Port	Terminal	Function
PA_0	33	N/A
PA_1	34	N/A
PA_2	35	Input for AUTO TUNING stop signal
PA_3	36	Input for memory IC's data
PB_{0-3}	37–40	Refer to Fig. 3.
PB_{0-3}	2–4	
PD_{0-3}	8–11	
PF_{0-3}	16–19	
PG_0	22	
PG_1	23	N/A
PG_2	24	N/A
PG_3	25	Output for muting pulse
PE_0	12	Clock output for PLL memory IC
PE_1	13	N/A
PE_2	14	Output for PLL latch
PE_3	15	Output for PLL and memory IC
PH_0	26	Outputs for memory IC address
PH_1	27	
PH_2	28	
PH_3	29	
PI_0	30	→C1 — Outputs for memory IC mode control
PI_1	31	→C2
PI_2	32	→C3

μPD2819C (IC602)

This is a CMOS LSI for the PLL frequency synthesizer designed for AM and/or FM radio/receiver.

Outline of μPD2819C:

18-pin molded DIP (dual-in-line package)

Data inputs are only three (3) because the data are put into the IC successively.

Has two input terminals for programmable divider and these terminals are selectable according to the program data (AM/FM).

Has an output (terminal 4) of 360 kHz for the controller.

Refer to the circuit diagram for its block diagram.

Table 2. Function of Terminals:

Terminal	Function
1	5 V power supply
2	5.76 MHz crystal oscillator
3	
4	Output 1 for 360 kHz clock signal
5	90 kHz test terminal 3
6	25 Hz clock signal output 2
7	unlock-detection terminal "1" (high) when PLL is locked, pulsative waveform when PLL is unlocked
8	Output terminal for phase comparator
9	Test terminal 1 for frequency comparison
10	Test terminal 2 for programmable divider's output
11	Input terminal for filter amp
12	Output terminal for filter amp
13	Grounding terminal
14	Input terminal 1 for programmable divider (AM)
15	Input terminal 2 for programmable divider (FM)
16	Shift register clock
17	Shift register data
18	Latch clock

Note: Terminals 16 – 18 are the input terminals for the program to decide the division ratio of the programmable divider, switching of terminals 11 and 12, and to decide the comparison frequency.

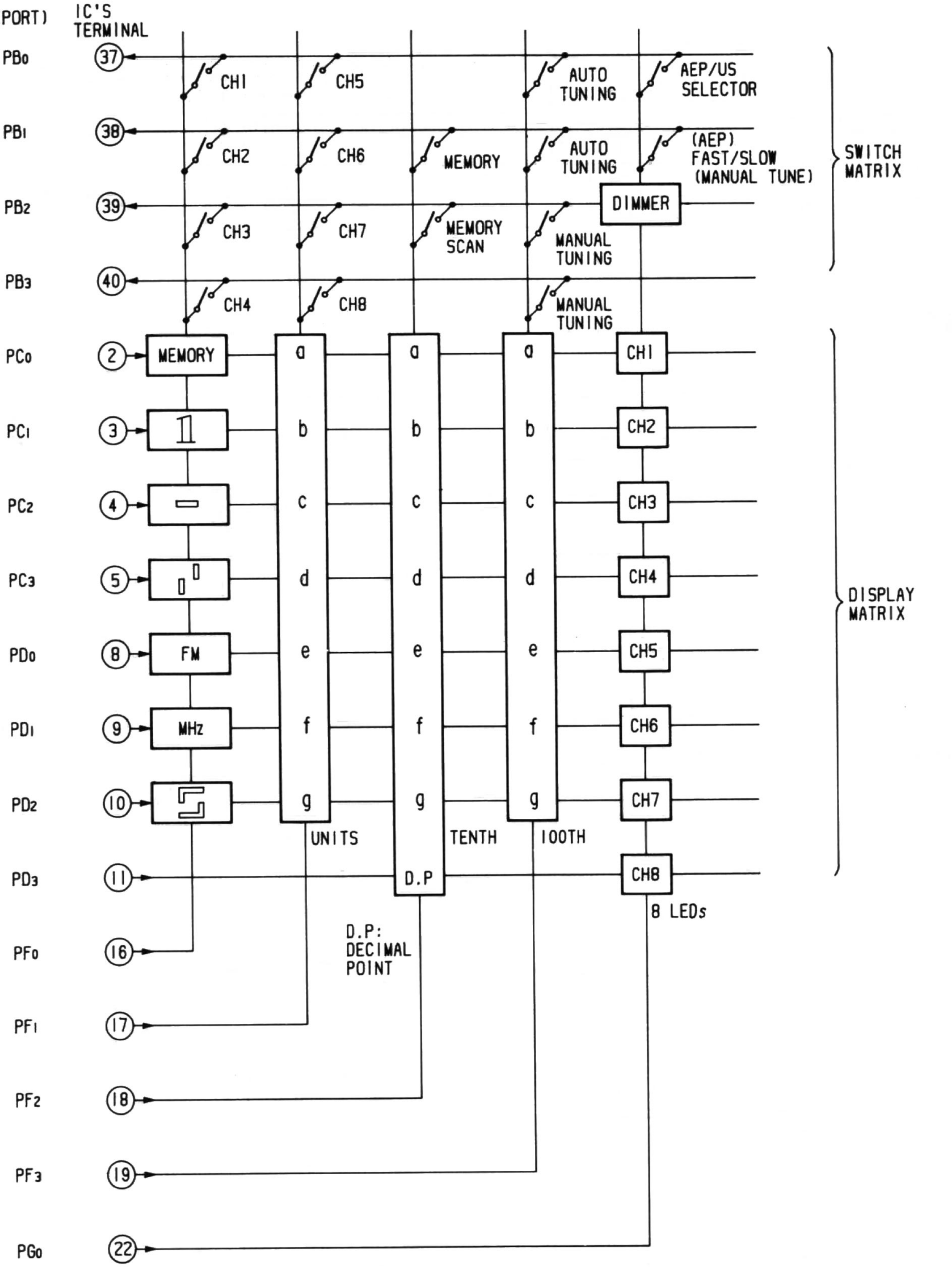
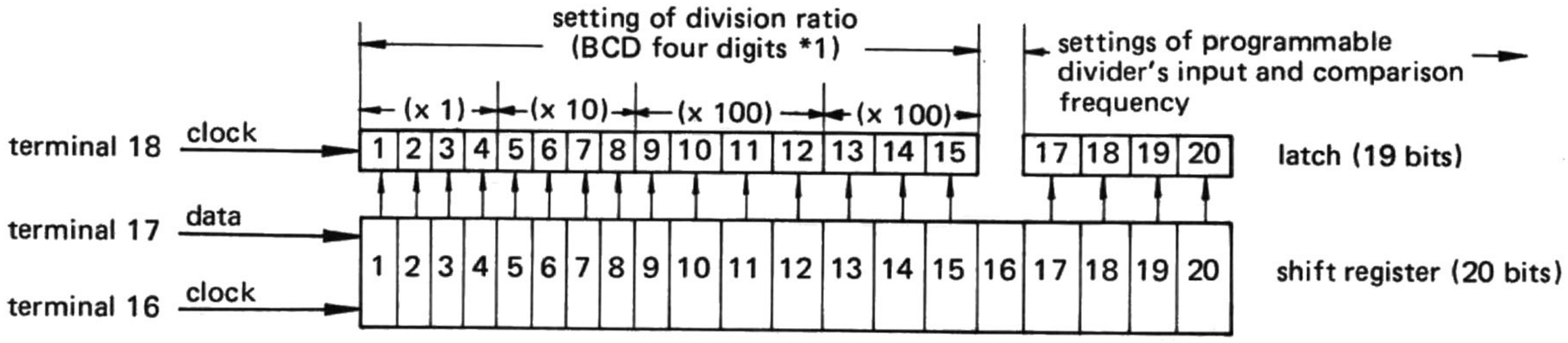
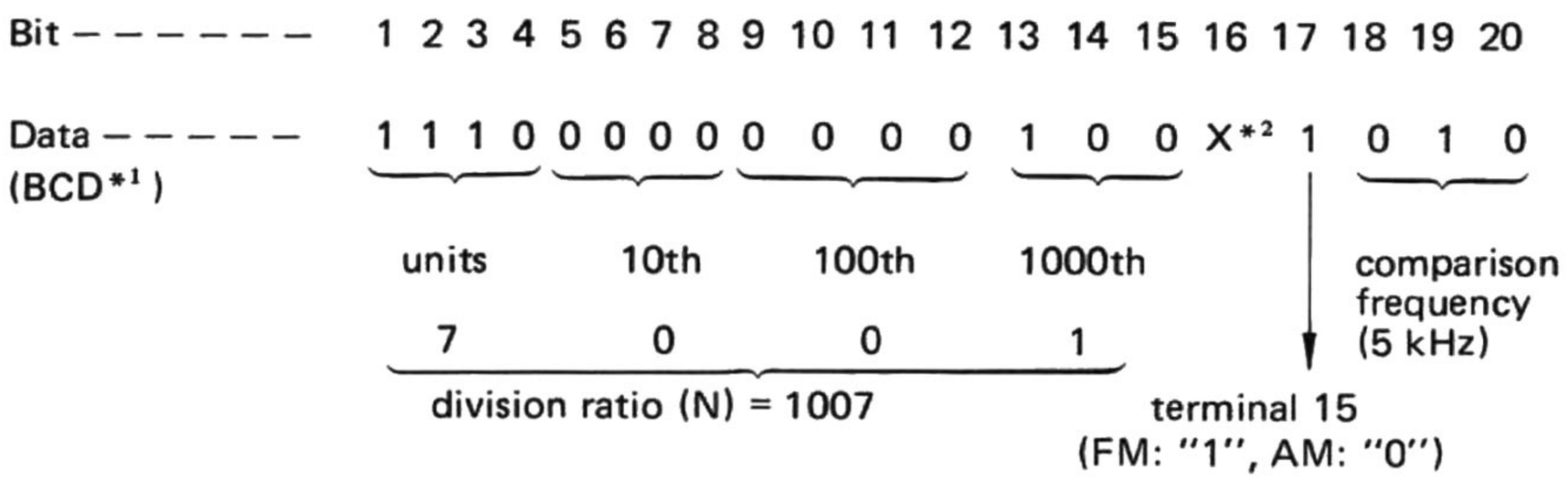


Fig. 3 Switches and Indication Matrix

Data Input Procedure from Microcomputer:



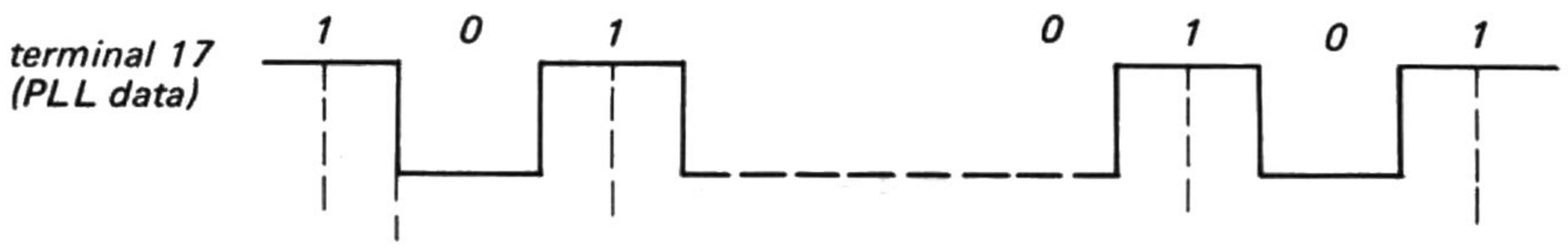
Example:



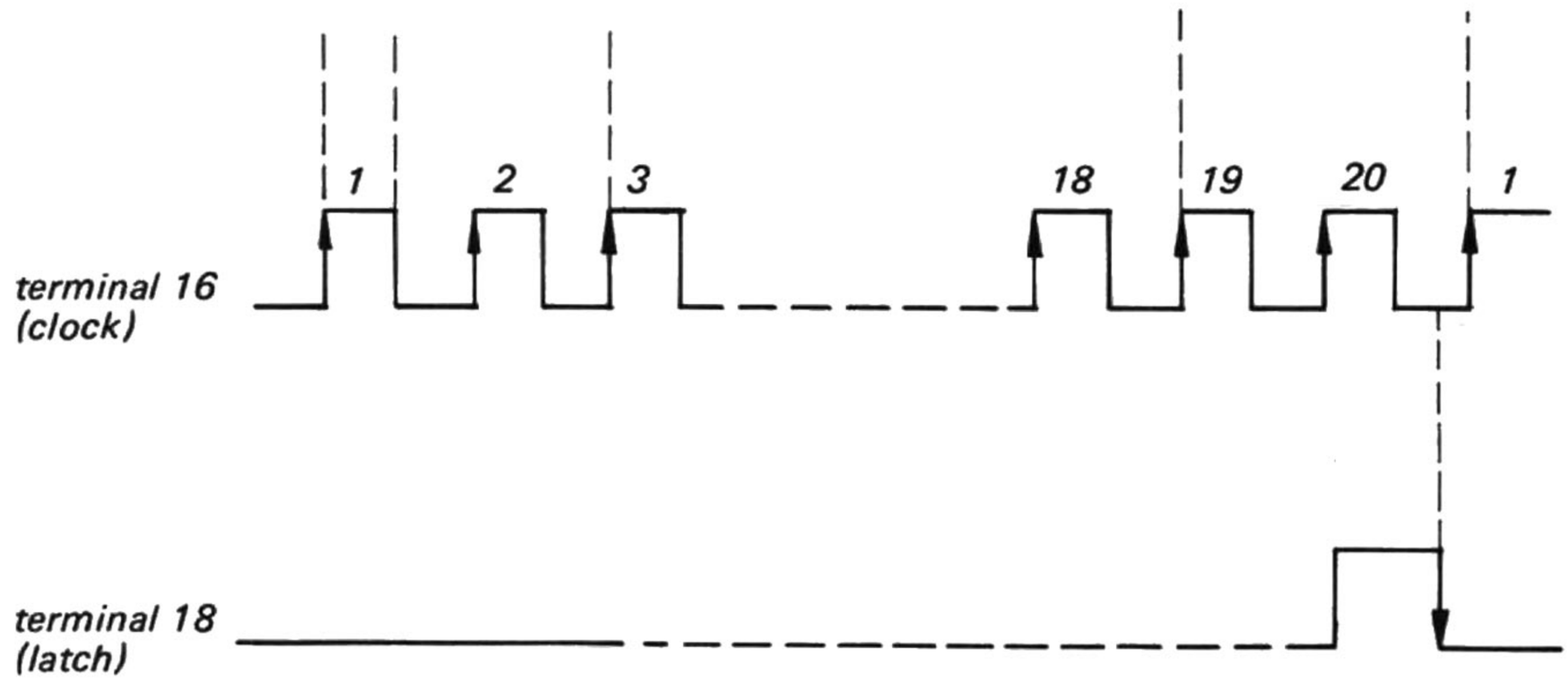
*1: BCD (Binary-Coded Decimal)
*2: 16th bit of the shift register is a dummy

Fig. 4

WAVEFORM EXAMPLES OF THE INPUT SIGNALS:



Date whether it is frequency, AM or FM is decided by the width and number of the pulse



With being latched started, the frequency is stabilized as a PLL system.

Note: The clock pulse of the shift register transfers data with its leading edge.
At the trailing edge of the latch pulse, the data is latched.

Fig. 5

MEMORY IC CX761 (IC605)

Outline of CX761:

(a) This is a non-volatile memory IC. Has 228 (14 words x 16 bits + 4 bits) non-volatile memory transistors built in, and works for reading, erasure and writing the data word.

(b) Because of being a non-volatile type memory, this IC maintains the memorized informations for a long time without a battery back-up after the power switch is turned off.

(c) Word address is done by the BCD inputs.

(d) Silicon-type P-channel enhancement MNOS IC construction.

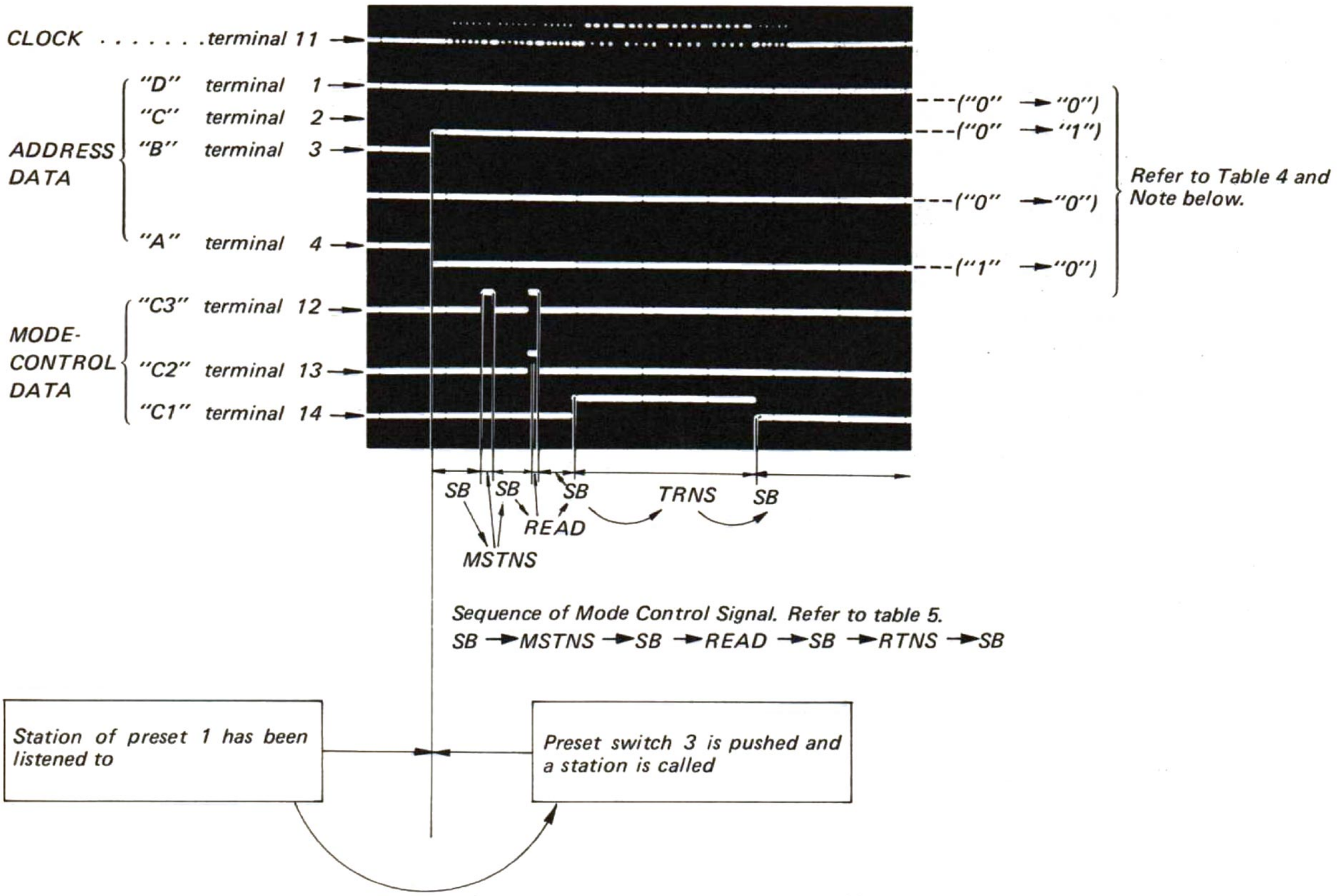
(e) 14-pin molded DIP casing.

Refer to the schematic diagram for the block diagram.

Table 3. Function of Terminals:

Terminal	IN or OUT	Function
1	IN	Word address D
2	IN	Word address C
3	IN	Word address B
4	IN	Word address A
5	IN	Power supply input
6	IN/OUT	Writing and erasure control inputs/memory-BUSY output
7	IN	Power supply input
8	IN/OUT	Inputs and outputs for test checkout
9	IN	Test signal
10	IN/OUT	Combined data inputs and data outputs
11	IN	Input for synchronous clock
12	IN	Input for mode control C3
13	IN	Input for mode control C2
14	IN	Input for mode control C1

An Example of Control Waveforms During Reading:



Note: Terminals 1 through 4 can be checked with a VOM.
"0" indicates 0 V (low level)
"1" indicates 5 V (high level)

Fig. 6

Table 4. Address Control Signals

ADDRESS / INPUT	0	1	2	3	4	5	6	7	8	9	10	11	12	13
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Note	last channel	preset 1	preset 2	N/A	preset 3	N/A	preset 5	preset 6	preset 4	preset 7	FM last channel	N/A	N/A	preset 8

Table 5. Mode Control Signals

MODE / INPUT	SB	RTNS	WTNS	WRT	MSTNS	ERS	READ	MCTNS
C1	0	1	0	1	0	1	0	1
C2	0	0	1	1	0	0	1	1
C3	0	0	0	0	1	1	1	1

Note:

SB: Standby

RTNS: Informations of the data register (relayed by the READ operation) are put out from the D I/O terminal

WTNS: Informations to be memorized are relayed to the data register from the D I/O terminal

WRT: Memorize the informations relayed by the WTNS operation in the designated address

ERS: Clears the informations memorized in the designated address

READ: Relay the memorized informations in the disignated address to the data register

MSTNS: The control signals which follow the MSTNS operation are processed in accordance with the station memory

MCTNS: Not applicable in this set (not used)

The Order of the Signals of the Read-mode Controls:

Address Disignation →SB (the clock is five-bit cycle) →MSTNS (one-bit cycle) →SB (five-bit cycle) →READ (one-bit cycle) →SB (five-bit cycle) →RTNS (sixteen-bit cycle) →SB (five-bit cycle)

The Order of the Signals of the Write-mode Controls:

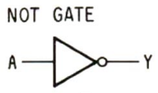
Address Designation →SB (the clock is five-bit cycle) →MSTNS (one-bit cycle) →ERS (external clock of approximately 100 msec) →SB (five-bit cycle) →WTNS (sixteen-bit cycle) →WRT (external clock of approximately 100 msec) →SB (five-bit cycle)

PLL (IC602), MEMORY (IC605), MICROCOMPUTER and their ASSOCIATED CIRCUITS:

(Refer to Fig. 8)

1) On the Symbols of the Digital Circuits used in This Set

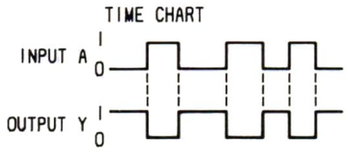
NOT GATE



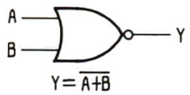
$Y = \bar{A}$

INPUT A	OUTPUT Y
0	1
1	0

TIME CHART



NOR GATE



$Y = \overline{A+B}$

INPUT A, B	OUTPUT Y
0 0	1
0 1	0
1 0	0
1 1	0

TIME CHART

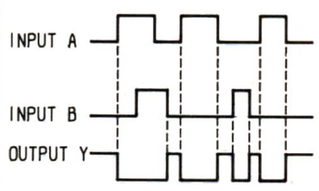


Fig. 7

2) When the Switches in Relation to the Writing, Reading are pushed (MEMORY and Preset Switches)

2-1)

(a) The base potential of Q604 becomes in 0 V and the collector potential in 5 V.

(b) This 5 V signal is applied to the NOT circuit (IC603), and terminal 6 of the memory clock IC604 becomes in 0 V.

(c) The clock signal is put out from terminal 12 of the microcomputer IC606 (route ②). This clock signal is applied to terminal 12 of the clock memory IC604 (Ⓐ), and the pulse output signal ④ is obtained at terminal 11 of IC604.

(d) The pulse output signal ④ is applied through the NOT circuit to terminal 11 of the memory IC605 (route ③).

(e) When the pulse signal is applied to terminal 11 of IC605, the clock generator in IC605 oscillates synchronizing with the pulse.

(f) When the clock signal is generated in IC605, writing and reading controls are performed, synchronizing with the clock signal, in IC605.

2-2)

(a) The pulse signal generated in step c of (2-1) above is applied through the NOT circuit IC603 to terminal 16 (shift register's clock terminal) of the PLL IC602 (route ③).

(b) The PLL IC602 reads out the microcomputer's data at the leading edge of the clock signal.

(c) By reading out the microcomputer's data, the division ratio of the program divider and the comparison frequency are decided in IC602.

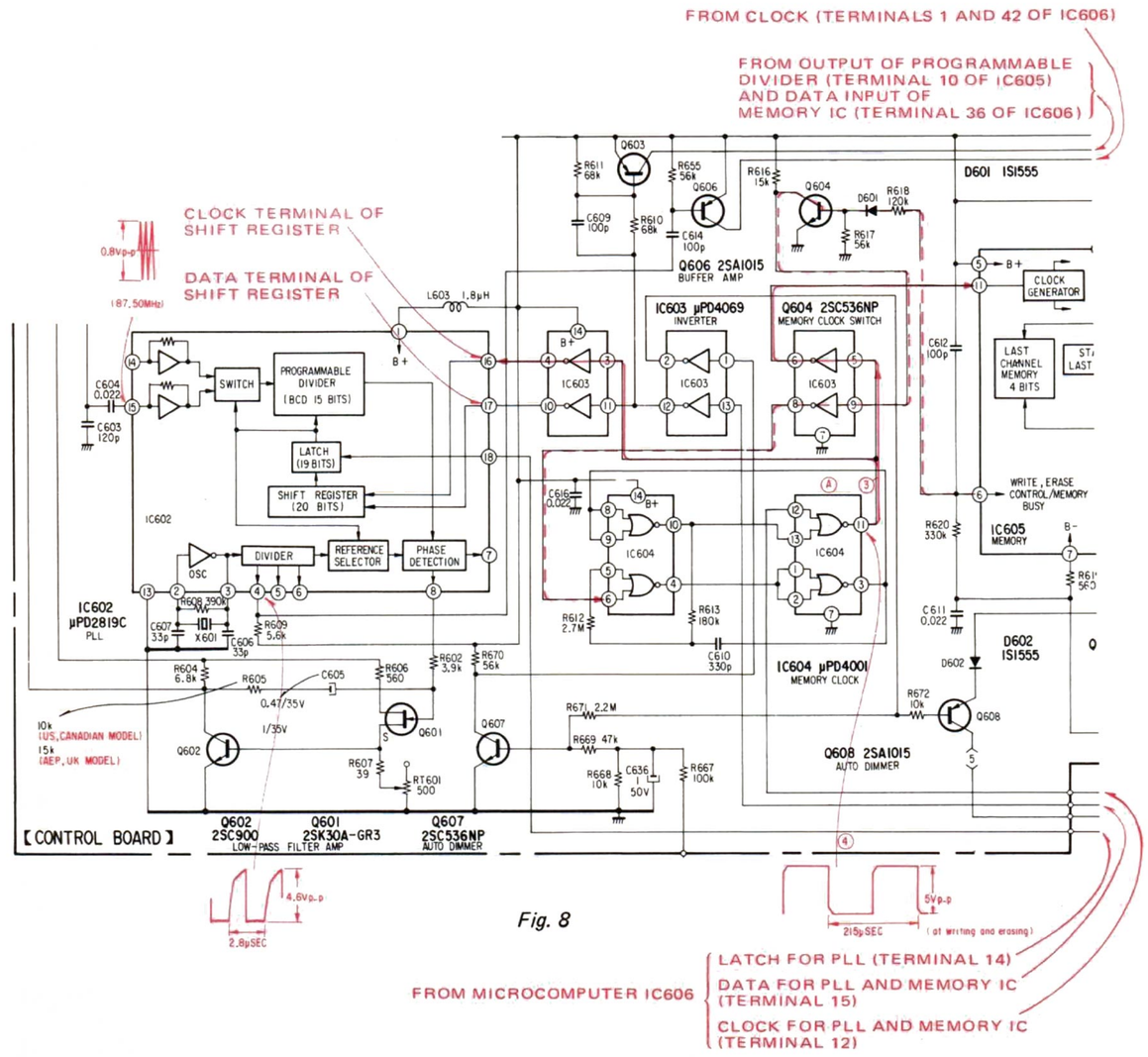


Fig. 8

Microcomputer IC606 and Its Associated Circuits:

1) Clock Conversion Circuit (Refer to Fig. 9):

The 5.76 MHz reference signal generated in IC 602 becomes through the divider in 360 kHz and is applied to the microcomputer. Before the 360 kHz signal goes from IC602 to IC606, a voltage conversion is needed because the low levels of both of them are greately different from each other (high levels are the same). The low level of IC602 is the ground potential (0 V), while that of IC606 is in the range of −1 V to −10 V. Q606 works as the voltage converter.

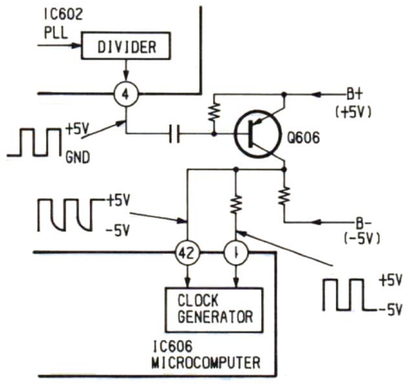


Fig. 9

2) Reset Signal (Refer to Fig. 10):

(a) This is the signal to be used to start the CPU right after the power switch is turned on or to reset the CPU to the initial condition freely. This reset signal (high level) is applied to terminal 7 of the CPU IC606. On receipt of the reset signal, the contents in the programmable counter (PC) and instruction register (IR) are cleared. Accordingly, the reset signal is released (reset: low) and the CPU starts operation from the address zero, i.e., location "0".

(b) The reset signal shapes the leading and trailing edges through a part of IC402 by utilizing the power-supply muting signal. Then the shaped reset signal is voltage-converted by Q403.

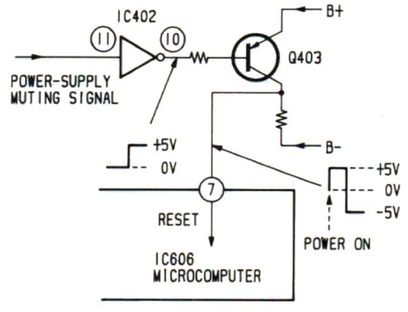


Fig. 10

3) AUTO TUNING Stop Signal (Refer to Fig. 11):

(a) In the auto-scanning mode, the scanning is disabled on receipt of a signal which level is higher than the muting level.

(b) To stop the auto scan, PA_2 (terminal 35 of IC606) is made to "high" level (+5 V).

(c) Q402 is the switching transistor to make the +5 V auto-stop signal and it turns on with 0 V input signal.

(d) Q401 receives a signal from the gate-circuit's muting diode D201 in the tuner section and drives Q402.

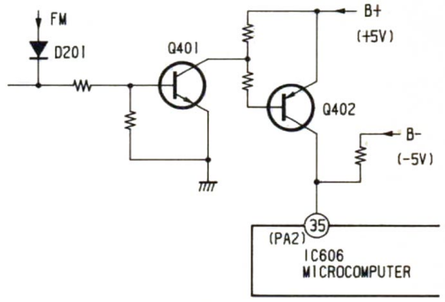


Fig. 11

4) Muting Circuit (Refer to Fig. 12):

This muting circuit operates with each of the following muting-control signals.

(a) Control Signal from Power Muting Q407: Muting operation is made when the power switch is turned on and off.

(b) Control Signals from FM-IF/DET Section of IC201:

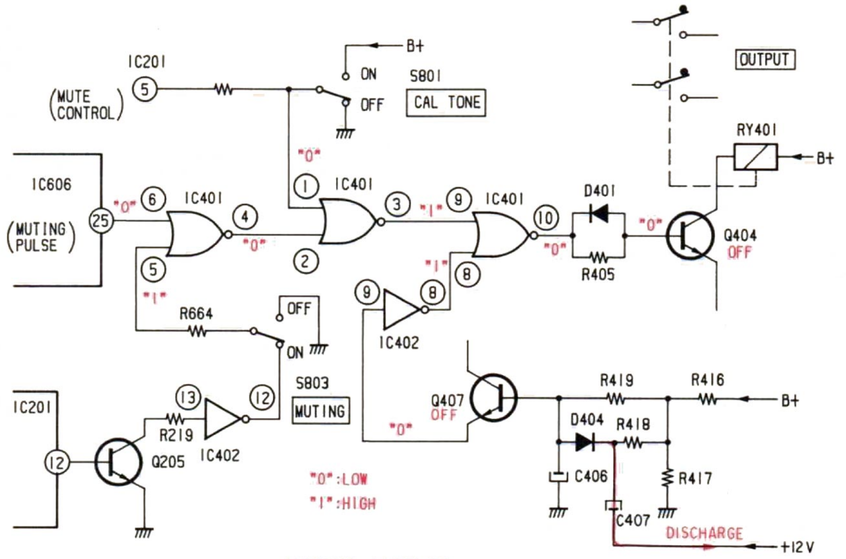
(b-1) Muting is made by detecting a DC voltage from the S-curve of the detector during the detuned condition.

(b-2) Muting is made by the level detection which detects the signal-to-noise ratio of the carrier when receiving weak signals.

(c) Control Signal from PG_3 (terminal 25 of the microcomputer IC606):
Muting is made by the high-level pulse output signal from PG_3 of IC606 during the receiving-signal changing.

4-1) Mutings during Power Switch Turning on and off (Refer to Fig. 12):

When the power switch is turned on, the power-supply muting transistor Q407 is turning off for about two seconds during which Q406 is charged up. When the power switch is turned off, C407 discharges rapidly. The base potential of Q407 is forcibly pulled to become more negative due to the discharging route through D404, and Q407 turns off as in the power switch is turned on, and thus its emitter potential becomes 0 V. Accordingly, the base potential of the relay driver Q404 becomes 0 V and Q404 turns off. When Q404 turned off, the reed relay RY401 also turns off and the output lines are cut off by the relay switches, thus the pop noise is muted at the OUTPUT jacks when the power switch is turned on and off.

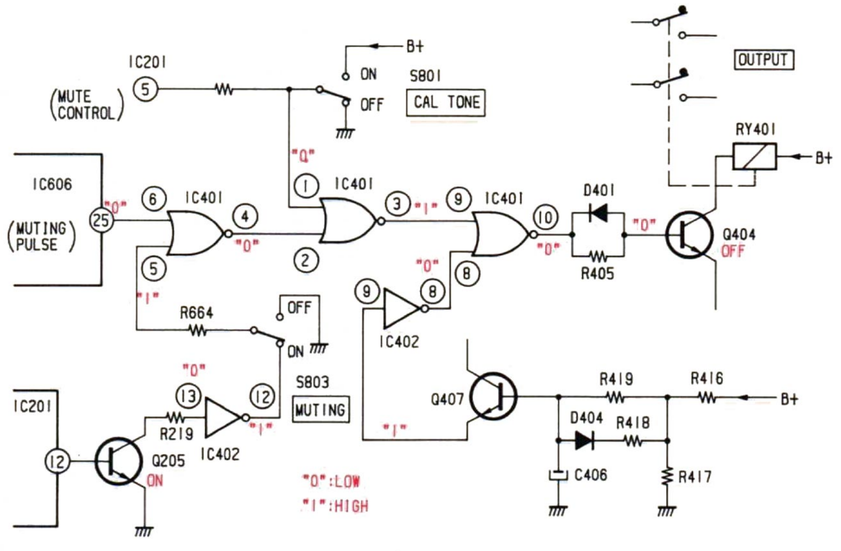


—MUTING CIRCUIT—

Fig. 12

4-2) Mutings during Detuned Condition and Weak-Signal Reception (Refer to Fig. 13):

When the set is detuned and receiving weak signals, a high-level signal is put out from terminal 12 of the FM-IF/DET IC201. This high-level signal is applied to the base of the muting transistor Q205, and Q205 turns on. When Q205 turns on, the collector potential of it becomes 0 V. Now "0" (low level) signal is applied to terminal 13 of IC402 and this signal is then applied through IC401 to the base of the relay driver Q404. This results in the turning off of Q404 and RY401, and no sound comes out from the OUTPUT jacks.

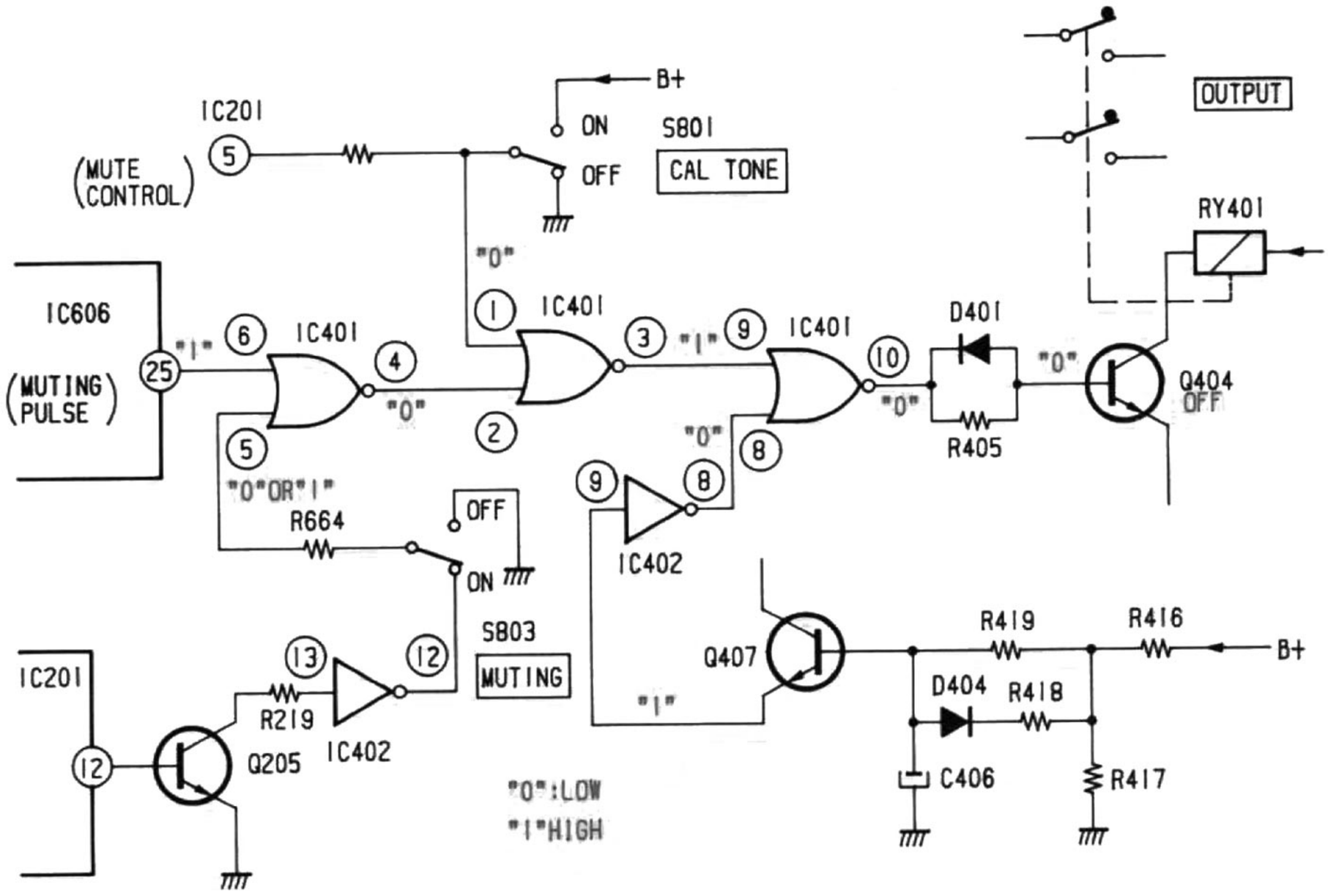


—MUTING CIRCUIT—

Fig. 13

4-3) Muting during Changing Receiving Frequencies (Refer to Fig. 14):

When the receiving station is changed by the preset switch, a high-level signal for muting is put out from terminal 25 of the microcomputer IC606 and is applied to terminal 6 of IC401. Terminal 4 of IC401 then becomes in "0" state, and thus the output signals are muted like in 4-2) above.



—MUTING CIRCUIT—

Fig. 14

CAL TONE CIRCUIT (Refer to Fig. 15):

This is an oscillator circuit using inverters for the record-level calibration purposes. This circuit is controlled by the signal applied to terminal 1 of IC402. When the signal at terminal 1 is high level, this circuit oscillates. When it is low, the circuit does not oscillate.

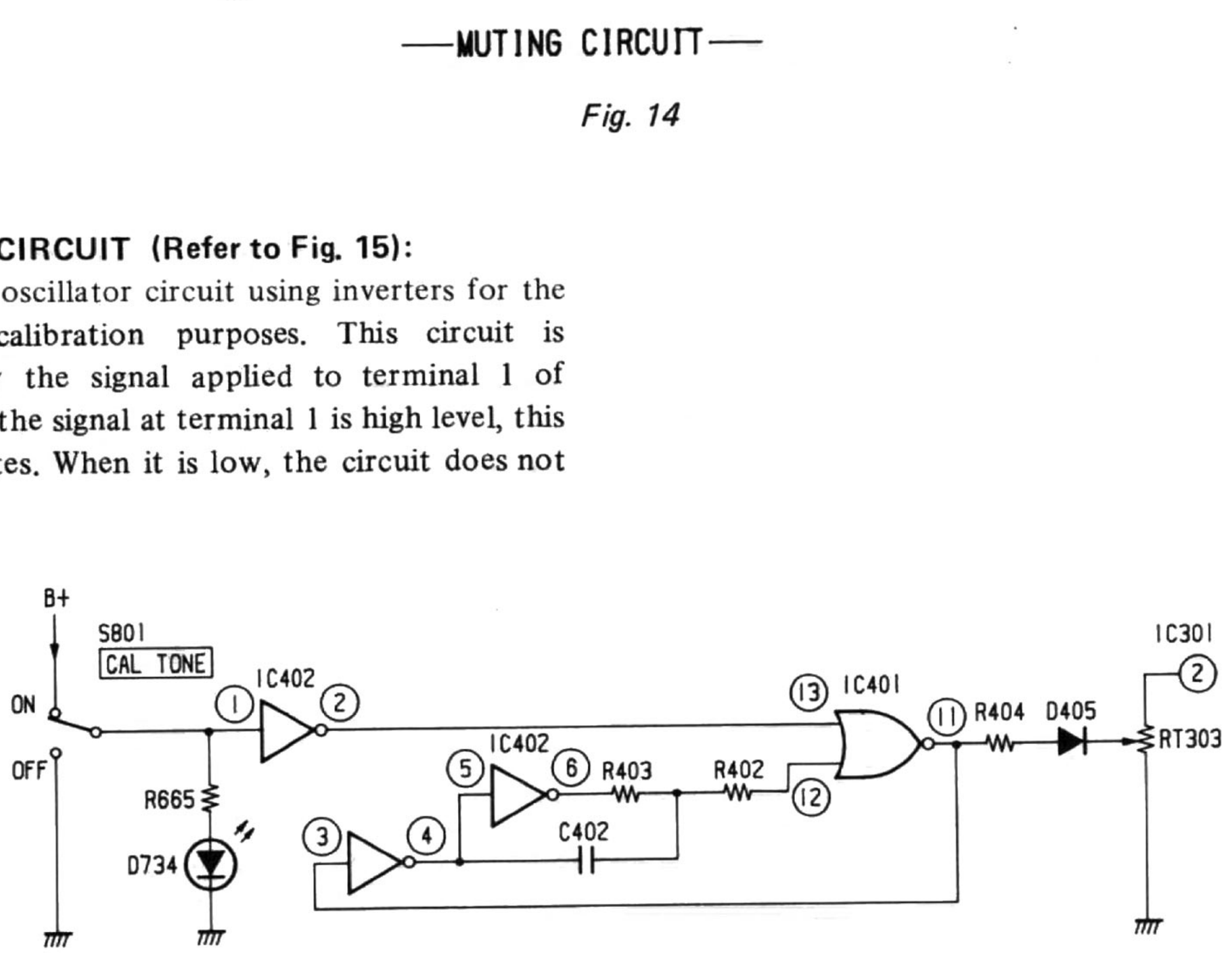


Fig. 15

DISPLAY FUNCTION OF MICROCOMPUTER IC606:

The display of this set is the dynamic light-up system. The microcomputer directly drives the display tube and the receiving frequency is displayed.

(a) Operating fundamental frequency is approximately 145 Hz (approximately 7 msec).

(b) Pulse width of the segment-drive pulses in more-lighter surroundings is approximately 1 msec and in more-darker one is approximately 0.5 msec.

Note: The eight LEDs of the preset frequency indicator are not affected by the surrounding light.

Fig. 16 shows the timing chart when receiving 96.30 MHz at 5 of the preset tuning switch. Also refer to Fig. 3 on page 7.

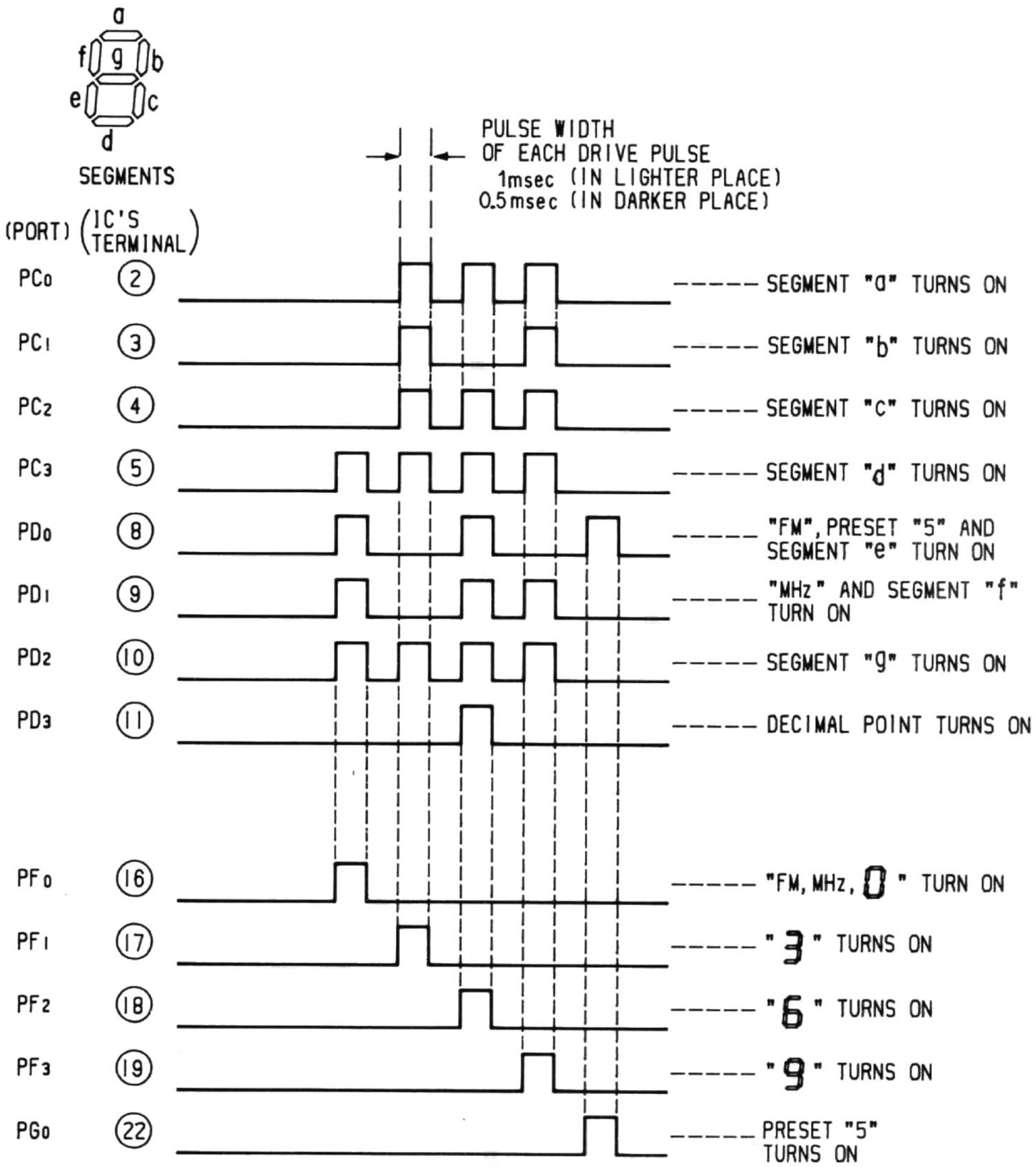


Fig. 16

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