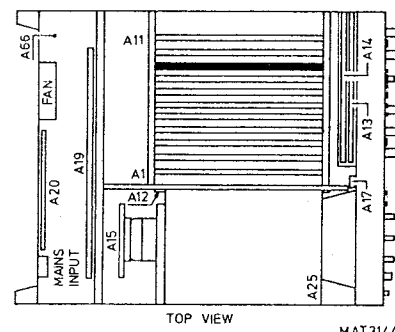


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8.9.1 General information

The DPU (Data Processing Unit) forms together with the DPU control (unit A8) a fast Data Processor. It is recommended to read first chapter 8.8.1 and 8.8.2 before reading chapter 8.9.2.

8.9.2 Circuit description

The DPU consists of the following parts:

- buffer
- register I
- complemeter
- adder
- register III
- overflow detection
- reflection suppression
- shift register
- limit detection
- register II
- pretrigger ram
- average ram
- flag ram
- flag handler

All these parts, excepted the adder and the overflow detection, are interconnected via the 16 bits wide DPU data bus (DADB00...15).

The BUFFER is a bidirectional data buffer (D1203, D1204 and D1206). To convert the 12 sample data bits to 16 DPU data bits SADB11 is applied to DADB11...15.

Ten processed sample data bits (SADB00...09) are applied to the display memory (unit A4).

When OTDIAD is low, data are transferred from the ADC (unit A11) to the DPU. When OTDIAD is high LEDP is high, data is transferred from

the DPU to the display memory. When OTDIAD is high and FBRY is high, data is transferred from the DPU to the Feedback DACs on the Management unit A25.

REGISTER I (D1216 + D1217) is a resettable latch, which is clocked by CKDUR1. It is used for various latching functions.

The COMPLEMENTER (+/-) complements data (D1211...D1214). It is used for subtractions with the adder.

Because the DPU calculates in two's complement notation, after complementation 1 should be added to get the correct negative number. This is done by the C0 signal on the carry input of the adder (D1218 pin 7).

The ADDER (D1218, D1219, D1221, D1222) adds the data from the complementer and register I.

The carry signal at pin 9 of D1222 can generate the CYOT signal via some logic (D1223).

REGISTER III (D1224 + D1226) is a latch, that latches the output result of the adder. It is clocked by CKDUR3.

The OVERFLOW DETECTION (D1231 and associated components) latches on CKDUR3 an overflow bit from D1228 pin 3 and a sign bit from D1222 pin 10 in D1231. So the two bits belong to the data that is clocked in register III. The table below shows which overflow is selected:

SLOFAD	ENOFD	Overflow from
X	0	always "1"
0	1	ADDER
1	1	ADC

Via the logic in D1227 the OTDI3 signal enables whether register 3 by OTEN3-LT or the reflection suppression by OTENRSLT, depending on the presence of overflow.

D1254 decodes the OEDU00 and OEDU01 signals to register control signals, which are active when RDDURM is low.

The REFLECTION SUPPRESSION (D1236...D1239) puts data on the DPU data bus when an overflow occurs, instead of Register III. It consists of a multiplexer, that selects 0000 0000 0011 1111 or 1111 1111 1100 0000, depending on the sign bit from D1231 pin 8.

This circuit prevents the arise of reflection of the input signal in the bottom of the display when high input voltages cause overflow in the display amplitude.

The same is valid in the top of the display with high negative input voltages.

The SHIFT REGISTER (D1242 + D1243) reads data from the DPU data bus, shifts them (left or right) and writes them back to the DPU data bus. This is used for multiplication or division by factors which are a multiple of 2.

The contents of the shift register can be cleared by RSSR--LT, which is used to write zeroes to the DPU data bus.

The signals SFSR00 and SFSR01 determine the function of the register (shift left or right, load or hold) on the clock signal CKSR.

The LIMIT DETECTION detects whether DUBB04...11 are all zero or one. This means that the data on the data bus represents a number that is between -16 and +16. This is used for some calculations.

REGISTER II (D1207 + D1208) is a latch, which is used for the intermediate storage of calculation results. It is clocked by CKDUR2LT. When OTDI2 is low, the register writes its data to the DPU data bus.

The PRETRIGGER + AVERAGE RAM consists of two 8Kx8 rams (D1249 + D1251), forming together an 8Kx16 ram. The lower address range is used as a 4Kx16 pretrigger ram. The higher address range is used as a 4Kx16 average ram.

The addresses for the ram are generated by the address generator on the DPU control (unit A8).

The highest address bit of the ram (pin 2) determines whether the pretrigger or the average ram is selected.

In the pretrigger ram a data word consists of 14 data bits, a real sample flag bit and an overflow flag bit.

In the average ram a data word consists of 16 data bits.

The FLAG RAM consists of a REAL SAMPLE FLAG RAM and an OVERFLOW FLAG RAM. Each consists of a 4Kx1 ram (D1252 and D1253), which contain the flags for the data in the average ram.

A real sample flag indicates whether a sample is a real taken sample or a sample that is obtained by means of interpolation between two real samples.

An overflow flag indicates an overflow of a sample. If one or both of two real samples behind each other have an overflow flag, all interpolated samples between them have an overflow flag.

The main functions of the FLAG HANDLER (D1241 and D1232...D1234) are given in the table below.

RDDURM	SLAM	Function of flag handler
0	0	Write flags (STRFL and STOFF) in pretrigger ram.
1	0	Read flags from pretrigger ram and write flags to D1233 and/or to display memory (unit A4) via D1232.
0	1	Write flags in flag ram (D1252 and D1253). Connect DUBB14 and DUBB15 to two MSB's of average ram (D1251 pin 18 + 19)
1	1	Read flags from flag rams to D1233 and to display. Connect two MSB's of average ram to DUBB14 and DUBB15.

The circuit consisting of D1233 and the gates behind, generates an overflow flag for interpolated samples if one of the real samples has an overflow flag.

Note: the overflow flags are not used in this instrument, but they can be read by an option.

8.9.3 Example of DPU operation

The following example describes in a simplified way the calculation of 7 interpolated samples between 2 real samples.

It is supposed that:

- a sweep of real samples is placed in the pretrigger ram.
- the distance between 2 real samples is 8 address locations.
- the intermediate locations have to be filled with interpolated samples.
- none of the real samples has an overflow flag.

The next actions are taken by DPU:

- 1: copy a real sample from the pretrigger ram to register II and to the shift register.
- 2: copy the next real sample to register I.
- 3: enable the register II outputs and activate CO (complement); the inverted first sample is applied to the adder.
- 4: now the adder subtracts the first sample from the second sample.
- 5: clock the sample difference in register III.
- 6: copy the sample difference to register I.
- 7: in the meanwhile the shift register has shifted left three times, which means that the sample value is multiplied by 8.
- 8: add the shift register contents and the sample difference.
- 9: clock the result (interpolated sample x8) in register III.
- 10: copy the contents of register III in the shift register.
- 11: by the enabled register III the next interpolated sample x8 is offered to the inputs of this register via the adder and the sample difference in register I.
- 12: clock this next interpolated sample in register III.
- 13: the shift register shifts right three times; the result is an interpolated sample.
- 14: copy the result to the pretrigger ram.
- 15: repeat steps 10 to 14 another six times for the remaining calculations of interpolated samples.

NOTES: - For obtaining maximum accuracy, the sample difference is not divided by 8, but the sample values are multiplied by 8.
 - The complex address generation for the pretrigger ram is done by the address generator on the DPU control.

8.9.4 Signal name list

UNIT A9

Signal name	Description	Signal source	Signal destination(s)
CKDUR1	Clock DPU register I	A8	-
CKDUR2LT	Clock DPU register II	A8	-
CKDUR3	Clock DPU register III	A8	-
CKF	Clock flags	A8	-
CKSR	Clock shift register	A9	A9
CO	Complement	A8	-
CSDURM	Chip select DPU ram	A8	-
CSF	Chip select flags	A9	A9
CYOT	Carry out	A9	A12-A8
DUAB00...11	DPU address bus 00...11	A9	-
DUDB00...15	DPU databus 00...15	A9	A9
ENOFD	Enable overflow detection	A8	-
ENPM--LT	Enable pretrigger memory	A9	A9
FBRY	Feedback ready	A8	-
LEDP	Latch enable display	A8	-
OFAD	Overflow ADC	A11	-
OFDP	Overflow display	A9	A12-A4, A12-A8
OTDI2	Output disable DPU register II	A9	A9
OTDI3	Output disable DPU register III	A9	A9
OTDIAD	Output disable ADC	A8	-
OTDISR	Output disable shift register	A9	A9
OEDU00	Output enable DPU 00	A8	-
OEDU01	Output enable DPU 01	A8	-
OTENRSLT	Output enable reflection suppression	A9	A9
OTEN3-LT	Output enable DPU register III	A9	A9
OTLD	Output limit detection	A9	A12-A8
RDDURM	Read DPU ram	A8	-
RLDP	Real sample display	A9	A12-A4, A12-A8
RSDUR-LT	Reset DPU registers	A8	-
RSSR--LT	Reset shift register	A9	A9
SADB00...11	Sample data bus 00...11	A9+A11	A12-A4, A12- A5-A12-A25
SFSR00	Select function shift register 00	A8	-
SFSR01	Select function shift register 01	A8	-
SLAM	Select average memory	A8	-
SLOFAD	Select overflow ADC	A8	-
STOFF	Set overflow flag	A9	A9
STRLF	Set real sample flag	A8	-
UPCK08	Microprocessor clock 8 MHz	A6	-

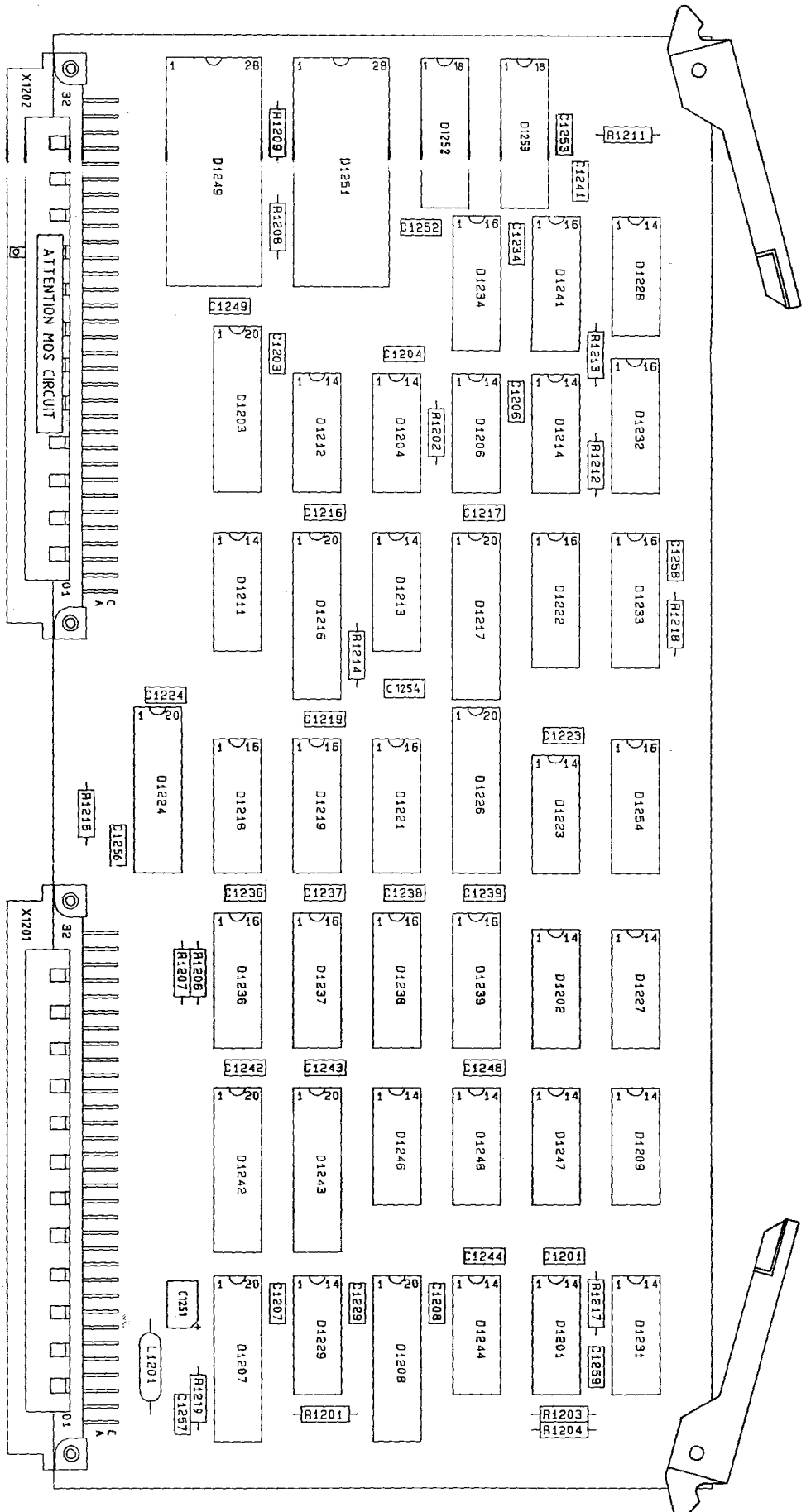
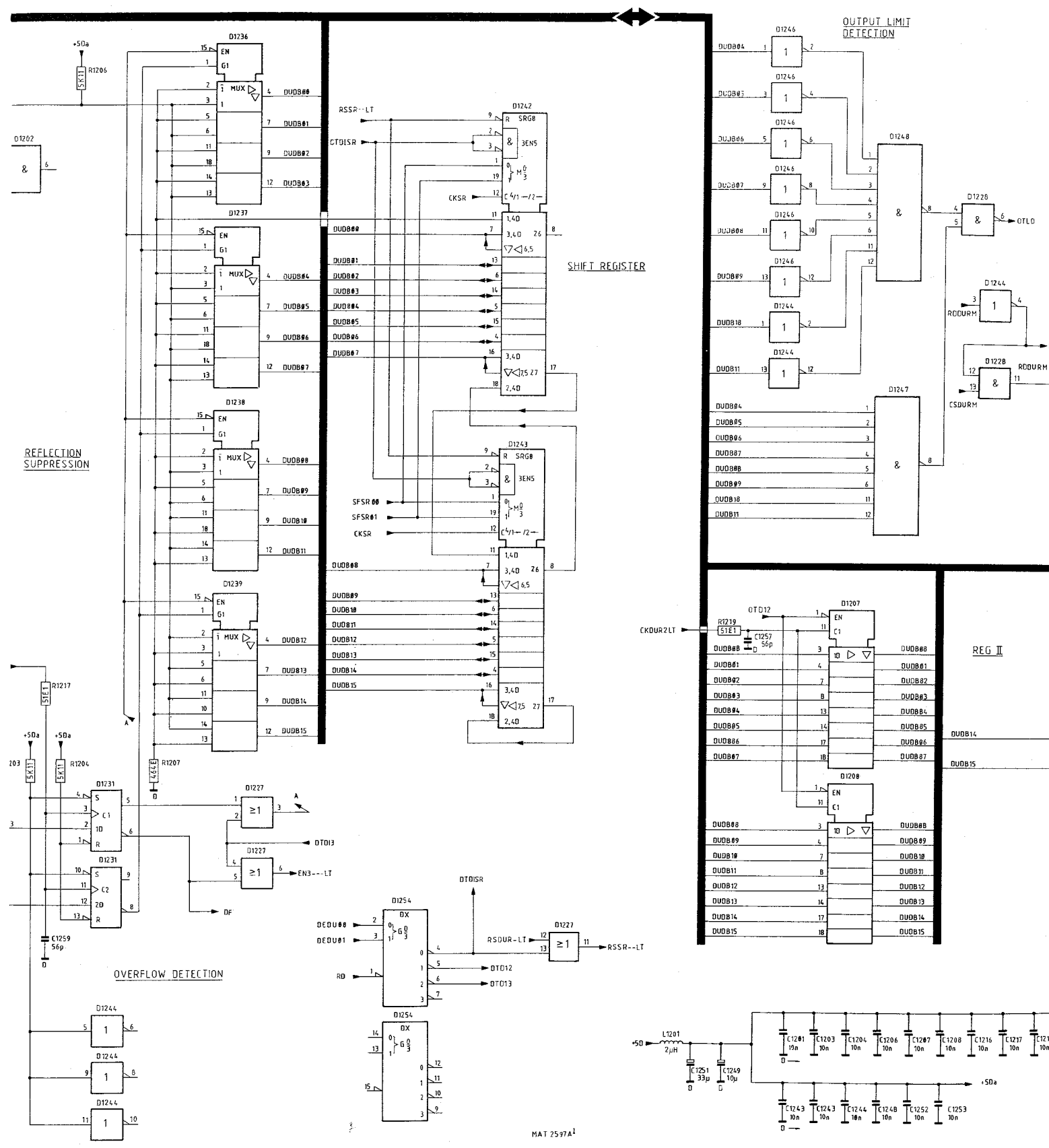
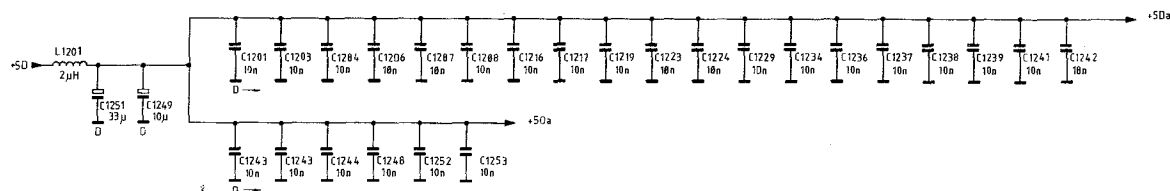


Figure 8.9.1 Unit A9 - DPU UNIT - P.C.B. lay-out.

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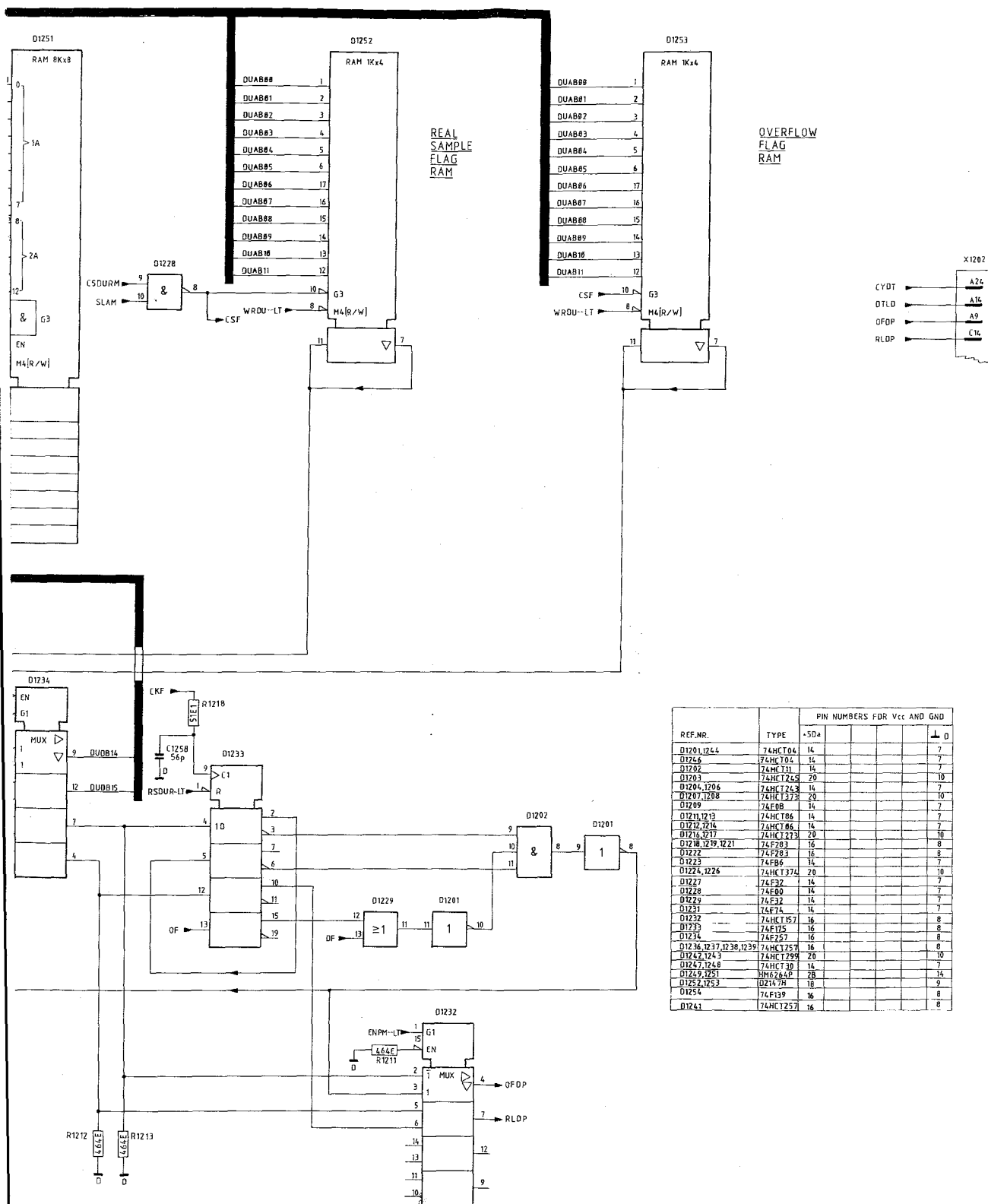


Figure 8.9.2 Unit A9 - DPU UNIT - circuit diagram.