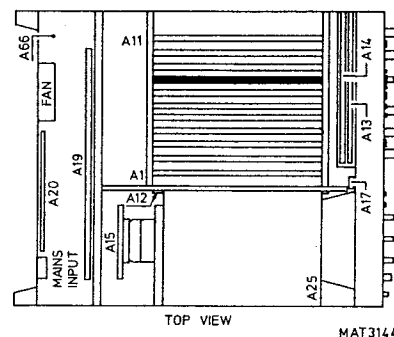


UNIT A8 - DPU CONTROL UNITCONTENTS

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## 8.8.1 General information

The DPU CONTROL forms together with the DPU (Data Processing Unit) a fast Data Processor with an instruction cycle time of 125 ns. The main function of the Data Processor is to accept sample data from the ADC, to perform calculations on it, to load the data in register R0 of the Display unit and to feed back sample data to the feedback DACs on the Management unit (see figure 8.8.1).

Other functions are:

- add samples of both channels in ADD mode
- invert samples of one or both channels
- linear interpolation
- flag handling (e.g. overflow)
- average calculations
- turning off feedback in eye pattern mode.

To perform these functions there are lines to the Acquisition Control Logic on unit A5, the ADC on unit A11, the Display Memory + Control on units A3 and A4 and the Feedback DACs on the Management unit A25. The Data Processor gets its programs from the microprocessor. When a program is finished or other DPU actions have to be reported, an interrupt to the microprocessor (IL02--LT) is generated. Normally it is rather difficult to check the proper operation of the Data Processor. Therefore it is recommended to use the "DPU test", which is in the diagnostic software (see chapter 11).

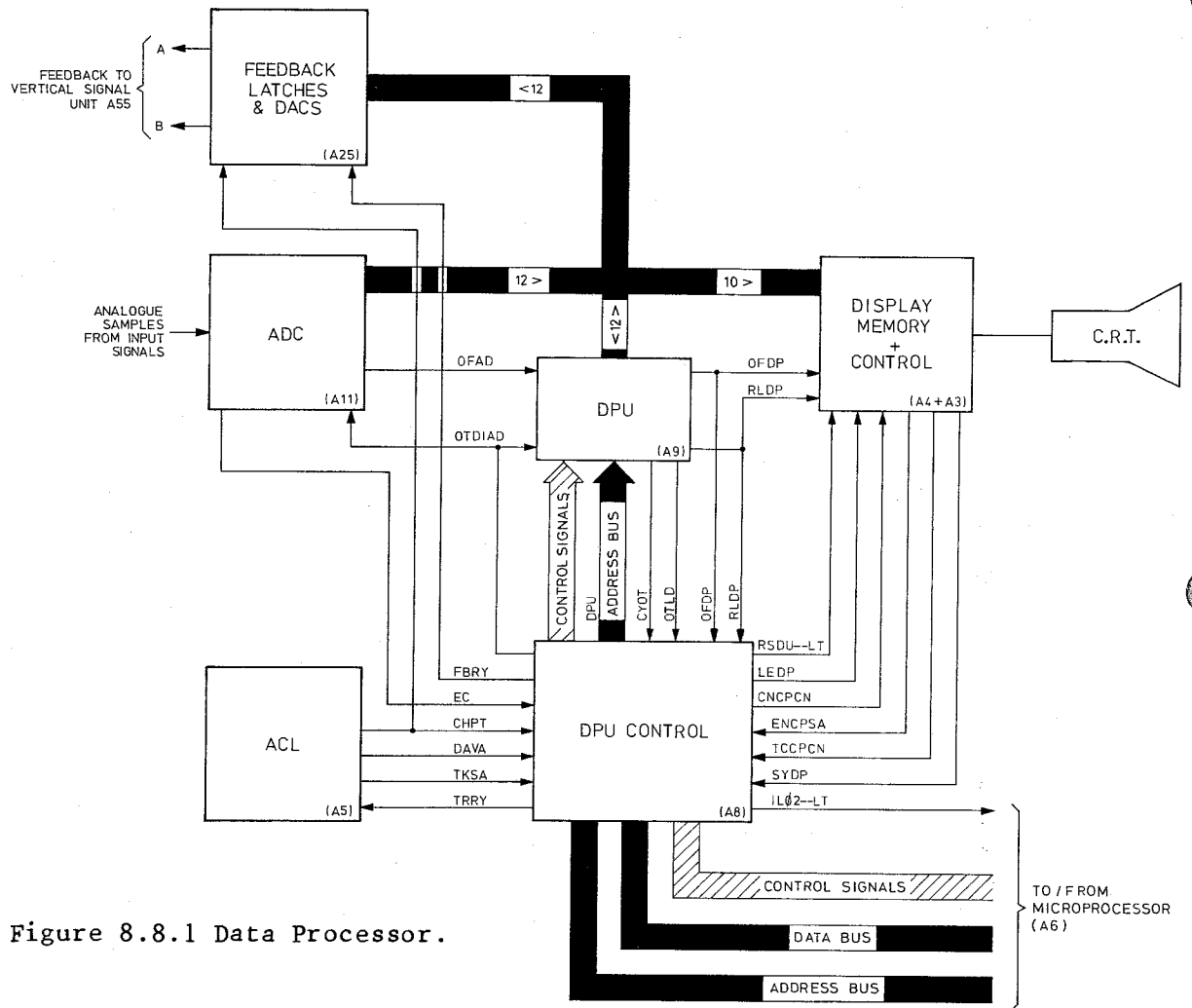


Figure 8.8.1 Data Processor.

MAT3087  
871223

### 8.8.2 Circuit description

The DPU (unit A9) performs the calculations on the sample data. To be able to do this, it receives a number of control signals and addresses from the DPU CONTROL.

These are derived from program words that are stored in the control memory.

The format of these 32 bit program words is defined as follows:

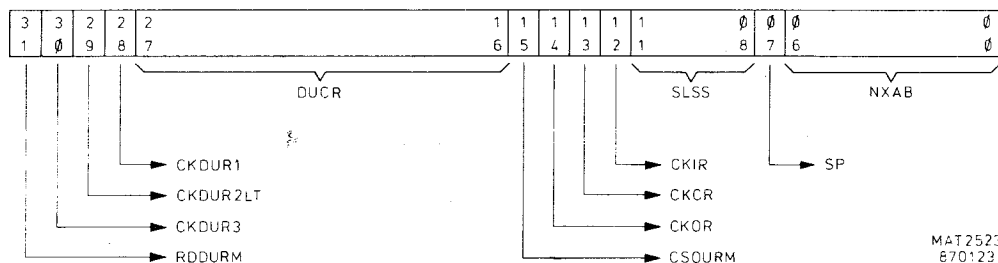
MAT2523  
870123

Figure 8.8.2 Program word format.

bits 00...06	are the 7 less significant bits of the address of the next instruction
bit 07	marks the end of a program
bits 08...11	selects statusbit in case of a conditional jump
bit 12	if set bits 16...27 are data for the instruction register
bit 13	if set bits 16...27 are data for the control register
bit 14	if set bits 16...27 are data for the offset jump register
bit 15	if set it generates the signal CSDURM for the DPU
bits 16...27	data for the instruction register or control register or offset jump register, depending on the status of bits 12...14
bits 28...31	if set they generate respectively the signals CKDUR1, CKDUR2LT, CKDUR3 and RDDURM for the DPU.

The control memory may contain one or more programs with a maximum length of 128 words (7 address bits).

The program which is selected depends on the 4 most significant address lines (bits 08...11).

The DPU CONTROL consists of the following parts:

- address decoder
- mode register
- start/stop logic
- status multiplexer
- address multiplexer
- control memory
- buffer
- pipeline register
- instruction register
- control register
- address generator

The ADDRESS DECODER, which mainly consists of IC D1401, decodes some address lines from the microprocessor to the select signals SLOT0...6. Because the logic on this unit is fast enough, the DATRAKLT signal can go low immediately when MYSL03LT goes low. IC D1424 generates a clock signal for the mode register when SLOT2 goes low and the SLAB signal when UPSL goes high. Furtheron this part contains some buffers for clock signals.

The MODE REGISTER (D1418) is an 8 bit latch that latches data from the microprocessor for the control of the start/stop logic.

The START/STOP LOGIC mainly consists of FPLS D1452 (Field Programmable Logic Sequencer). It generates a number of control signals depending on the status of its input signals.

Three outputs and the output of the status multiplexer are latched by IC D1458. The four outputs determine via the address multiplexer the four most significant address bits of the next instruction. If output pin 16 or pin 17 of D1457 goes low IL02--LT is generated via D1404. The microprocessor reads then via D1423 the status of both outputs. The going low of pin 17 marks that the DPU has finished its program.

The STATUS MULTIPLEXER consists of two 1 of 8 multiplexers (D1402 and D1403), which form together a 1 of 16 multiplexer.

The status signal that is selected is determined by the SLSS00...03 signals from the pipeline register b.

The ADDRESS MULTIPLEXER (D1409, D1411 and D1412) is a 12 bit multiplexer of which 11 bits are used.

When a DPU program is executed SLAB is low. NXAB00...NX06 and four output signals of D1458 are selected. The address of the next word in the control memory is determined by the 7 less significant bits of the current word and the signals SS1, IS, CL0 and CL1.

When a DPU program is loaded in the control memory by the microprocessor, SLAB is high. The address where the word is loaded is determined by the address selected by the microprocessor.

The CONTROL MEMORY is a 2048 x 32 ram. It is built with four 2048 x 8 ram's (D1426...1429). SLOT0 is the write signal for the lower 16 bits of a word, SLOT1 is the write signal for the higher 16 bits of a word.

When a DPU program is executed both are high, which results in the read status of the ram. The data on the DUIR bus are determined by the address on the IRAB.

The buffer is a 32 bit buffer (D1413, D1414, D1416 and D1417) between the microprocessor data bus and the DUIR bus. It separates data on both buses when a DPU program is executed.

When a DPU program is loaded, data from the microprocessor are transferred to the control memory by the SLOT0 and SLOT1 signals, which also control the control memory.

The PIPELINE register is a 32 bit register (D1431...1434), which holds the current instruction, while the next instruction is fetched from the control memory. It is clocked by CKPL, which is generated by the start/stop logic.

At the outputs of the register the definition of the program word can be recognized.

The INSTRUCTION REGISTER (D1441 + D1442) is a 12 bit latch, that latches 12 signals for the DPU. It is clocked by CKIR, which is derived from bit 12 of the program word via D1459.

The CONTROL REGISTER (D1438 + D1439) is a 12 bit latch, that latches 12 signals, which are mainly used on this unit. It is clocked by CKCR, which is derived from bit 13 of the program word.

The ADDRESS GENERATOR generates addresses for the pretrigger ram, the average ram and the flag ram on the DPU.  
It consists of the following parts:

- buffer
- offset jump register
- address register
- adder
- pretrigger counter
- multiplexer
- trigger address comparator

The BUFFER is a 12 bit buffer (D1421 + D1422), which latches data from the microprocessor. It is clocked by SLOT4.

When OTDIPR is low the data are put on the DPU address bus (DUAB00...11). DUAB00 is also led to the status multiplexer.

The OFFSET JUMP REGISTER (D1436, D1419 + D1437) consists of two parts. If OTENDT is low, D1436 and D1437 latch DUCR00...11, which is the offset jump. D1436 and D1437 are clocked by CKOR, which is derived from bit 14 of the program word. The output signals are applied to the adder.

If OTENDT is high DB08...DB15 are latched by D1419 on SLOT2. D1437 is reset.

The output signals of D1419 and D1437 are applied to the adder.

Due to the inverter D1406 either the outputs of D1436 or D1419 are enabled.

The ADDRESS REGISTER (D1443 + D1444) is a 12 bit latch, which latches data from the DPU address bus. It is clocked by CKAD. It can be reset by RSAD--LT.

The ADDER is a 12 bit adder, which adds data from the offset jump register and the address register. The carry signal (CYAA) is led to the status multiplexer.

The preset value is loaded from the DPU address bus by LDPRCNLT. The counter value is applied to the pretrigger address bus (PRAB00...11). When all counter bits are "1" TCPRCN is generated by D1404. It is led to the status multiplexer.

The MULTIPLEXER (D1449, D1451 and D1452) selects data from the adder or from the pretrigger counter. The data are applied to the DPU address bus.

When SLPRAB is low, the data from the adder are selected, otherwise data from the pretrigger is selected.

Because OTDIPR and OTDIMX are in antiphase (D1406 pin 3 and 4) either the buffer or the multiplexer writes data to the DPU address bus.

## 8.8.3 Signal name list

## UNIT A8

Signal name	Description	Signal source	Signal destination(s)
AB02...12	Address bus 02...12	A6+Option	-
CHPT	Channel pointer	A5	-
CKAD	Clock address register	A8	A8
CKCL	Clock cycle counter	A8	A8
CKCR	Clock control register	A8	A8
CKDUR1	Clock DPU register I	A8	A12-A9
CKDUR2LT	Clock DPU register II	A8	A12-A9
CKDUR3	Clock DPU register III	A8	A12-A9
CKDU08LT	Clock DPU 8 MHz	A8	A8
CKDU16LT	Clock DPU 16 MHz	A8	A8
CKF	Clock flags	A8	A12-A9
CKIR	Clock instruction register	A8	A8
CKOR	Clock offset jump register	A8	A8
CKPL	Clock pipeline register	A8	A8
CL0...1	Cycle 0...1	A8	A8
CNCPCN	Count copy address counter	A8	A12-A4
CO	Complement	A8	A12-A9
CSDURM	Chip select DPU ram	A8	A12-A9
CYAA	Carry address adder	A8	A8
CYOT	Carry out	A9	-
DATRAKLT	Data transfer acknowledge	A8+A3+A5+ A6+Option	A12-A6, A12-Option
DAVA--03	Data valid	A5	-
DB00...15	Data bus 00...15	A6+Option	-
DUAB00...11	DPU address bus 00...11	A8	A12-A9, A12-A4
DUCR00...11	DPU control register 00...11	A8	A8
DUIR00...31	DPU instruction register 00...31	A8	A8
EC	End of conversion	A11	-
ENCP	Enable copy	A8	A8
ENCPSA	Enable copy sample	A4	-
ENOFD	Enable overflow detection	A8	A12-A9
ENPRCN	Enable pretrigger counter	A8	A8
FBRY	Feedback ready	A8	A12-A9, A12-A5-A12-A25
IL02--LT	Interrupt level 02	A8	A12-A6, A12-A5
IRAB00...10	Instruction register address bus 00...10	A8	A8
IS	Initialisation	A8	A8
LDPRCNLT	Load pretrigger counter	A8	A8
LEDP	Latch enable display	A8	A12-A4
MYSL03LT	Memory select 03	A6	-

Signal name	Description	Signal source	Signal destination(s)
NXAB00...06	Next address bus 00...06	A8	A8
OEDU00	Output enable DPU 00	A8	A12-A9
OEDU01	Output enable DPU 01	A8	A12-A9
OFDP	Overflow display	A9	-
OTCM	Output comparator	A4	-
OTDIAD	Output disable ADC	A8	A12-A9, A12-A11
OTDIMX	Output disable multiplexer	A8	A8
OTDIPR	Output disable pretrigger	A8	A8
OTENDT	Output enable delta-t	A8	A8
OTLD	Output limit detection	A9	-
PRAB00...11	Pre-trigger address bus 00...11	A8	A8
RDDURM	Read DPU ram	A8	A12-A9
RLDP	Read sample display	A9	-
RSAD--LT	Reset address register	A8	A8
RSDU--LT	Reset DPU	A8	A12-A4
RSDUR--LT	Reset DPU registers	A8	A12-A9, A12-A4
SFSR00	Select function shift register 00	A8	A12-A9
SFSR01	Select function shift register 01	A8	A12-A9
SLAB	Select microprocessor address bus	A8	A8
SLAM	Select average memory	A8	A12-A9
SLOFAD	Select overflow ADC	A8	A12-A9
SLOT0...6	Select output 0...6	A8	A8
SLPRAB	Select pretrigger address bus	A8	A8
SLSS0...6	Select status 0...6	A8	A8
SP	Stop	A8	A8
SS	Status	A8	A8
SS1	Status 1	A8	A8
STRLF	Set real sample flag	A8	A12-A9
SYDP	Synchronize display	A3	-
TCCPCN	Terminal count copy address counter	A4	-
TCPRCN	Terminal count pre-trigger counter	A8	A8
TKSA	Take sample	A5	-
TRRY	Transfer ready	A8	A12-A5
UPCK08	Microprocessor clock 8 MHz	A6	-
UPCK16	Microprocessor clock 16 MHz	A6	-
UPDO	Up/Down	A8	A8
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-
UPSL	Microprocessor select	A8	A8

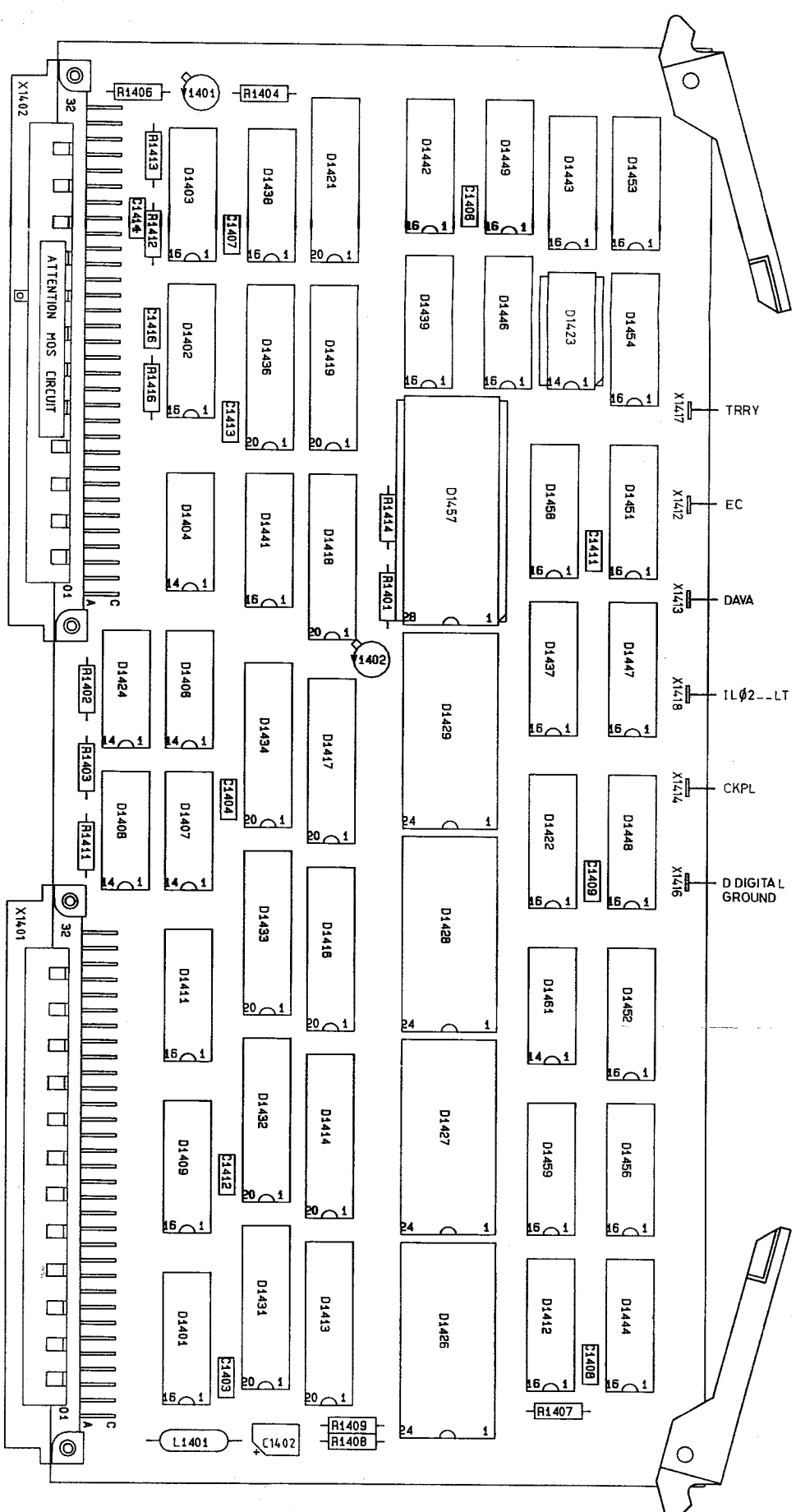


Figure 8.8.3 Unit A8 - DPU CONTROL UNIT - p.c.b. lay-out.

MA12537A  
880205



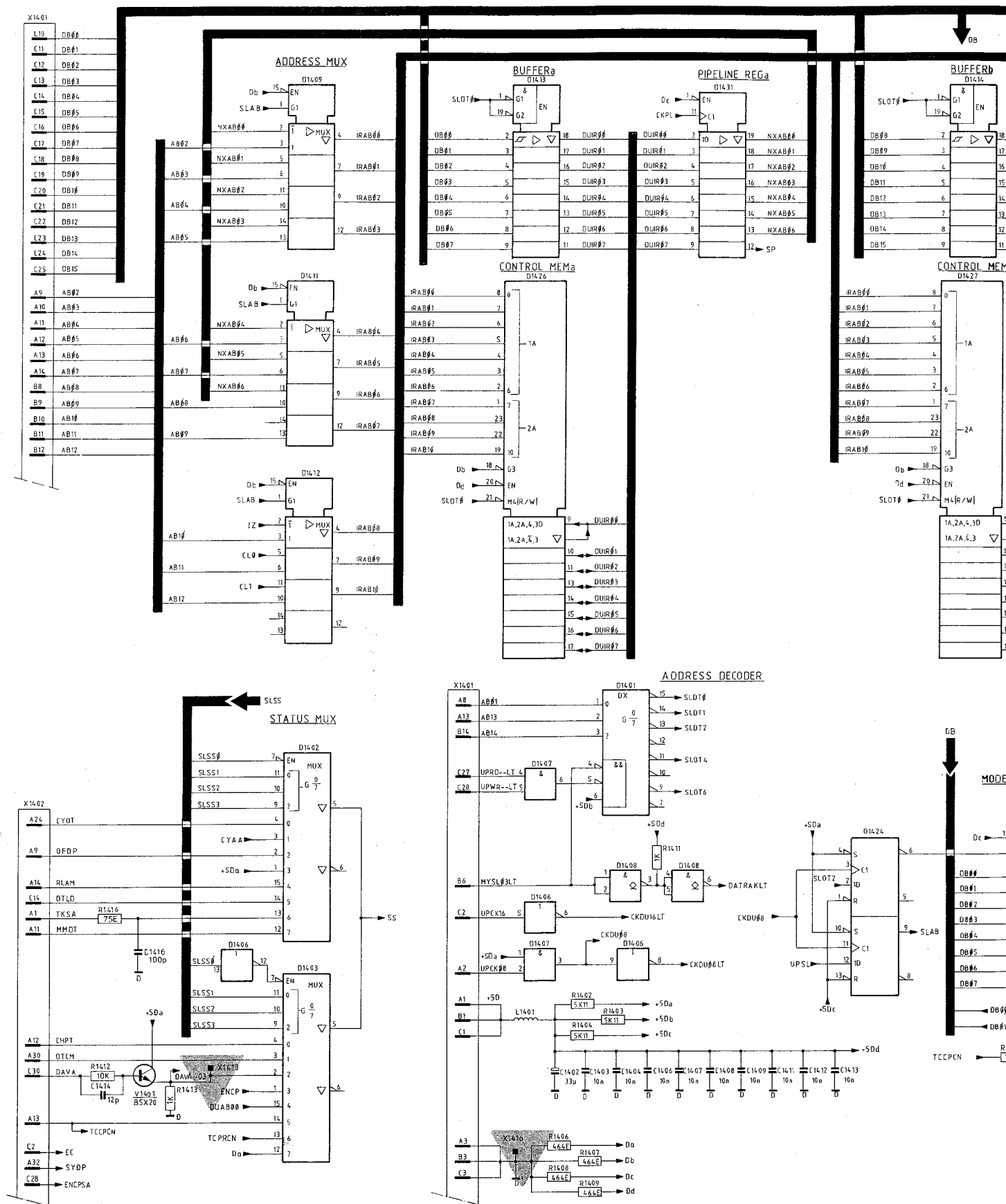


Figure 8.8.4 Unit A8 - DPU CONTROL UNIT - circuit diagram.

