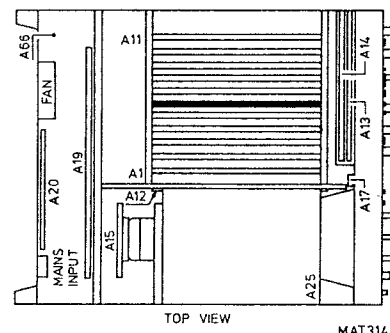


UNIT A6 - UP UNITCONTENTS

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8.6.1 General information

This unit mainly consists of a powerfull 68000 microprocessor configuration with EPROM, address decoders, I/O buffers and a clock generator. The microprocessor runs at a clock frequency of 8 MHz. A bus arbiter has been provided to allow a multiprocessor system, which is used when options are installed in the instrument. The microprocessor has an asynchronous bus structure with a 24 bit address bus and a 16 bit data bus.

Asynchronous means that the microprocessor waits for a "data acknowledge" signal from selected I/O circuitry, before continuing. This enables the microprocessor to handle different access times in I/O circuitry.

8.6.2 Memory map

Address (Hex)		
0000000	03FFFF	ROM0
0400000	07FFFF	ROM1
0800000	0BFFFF	Not used
0C00000	0FFFFFF	uP I/O
		Not used
C000000	CFFFFFF	I/O
D000000	D1FFFF	RAM0
		Not used
D200000	D3FFFF	Display RAM
D400000	D5FFFF	DPU RAM + I/O
D600000	D7FFFF	OPTION 2
D800000	D9FFFF	RAM1
DA00000	FFFFFF	Not used

Unit A6

Outside unit A6

I/O Select

MYSL01LT
Unit A5

MYSL02LT
Unit A4 + unit A3

MYSL03LT
Unit A8

MYSL04LT

MYSL01LT
Unit A5

Address (Hex)		
0000000	03FFFF	ROM0
0400000	07FFFF	ROM1
0800000	0BFFFF	Not used
0C00000	0FFFFFF	uP I/O
		Not used
C000000	FFFFFF	I/O
D000000	D1FFFF	RAM0
		Not used
D200000	D3FFFF	Display RAM
D400000	D5FFFF	DPU RAM + I/O
D600000	D7FFFF	OPTION 2
D800000	D9FFFF	RAM1
DA00000	FFFFFF	Not used

Unit A6

Outside unit A6

I/O Select

MYSL01LT
Unit A5

MYSL02LT
Unit A4 + unit A3

MYSL03LT
Unit A8

MYSL04LT

MYSL01LT
Unit A5

A number of I/O select signals select address ranges in the I/O part of the memory map, according to the following table:

Select signal	Selected address range	Used for
IOSL03LT	C00000-C1FFFFFF	Option
IOSL04LT	C20000-C3FFFFFF	Front units A13 + A14
IOSL05LT	C40000-C5FFFFFF	Display unit A3
IOSL06LT	C60000-C7FFFFFF	Not used
IOSL07LT	C80000-C9FFFFFF	Management unit A25
IOSL08LT	CA0000-CBFFFFFF	A.C.L. part unit A5
IOSL09LT	CC0000-CDFFFFFF	Not used
IOSL10LT	CE0000-CFFFFFFF	Option

The data acknowledge signal for the microprocessor is generated on this unit (A6) when an I/O select signal is active. When a memory select signal is active the data acknowledge signal is generated on the selected unit via a wired or open collector circuit (DATRAKLT).

8.6.3 Interrupts

Peripheral circuits can generate an interrupt to the microprocessor to ask for special actions. Each interrupt has a priority level according to the table below. The higher the interrupt number is, the higher its priority level is. Interrupts with a priority level which is lower than or equal to the priority level of the currently being handled interrupt are inhibited, until the higher priority level interrupt is handled.

Interrupt signal	Comes from
IL01--LT	Microprocessor unit A6
IL02--LT	DPU unit A9
IL03--LT	Front unit A14
IL04--LT	Option
IL05--LT	Display unit A3
IL06--LT	Not used
IL07--LT	Power 2 unit A20

The functions of the interrupts are:

IL01--LT	Comes every 40 ms. It starts a scan of the front panel keys and updates the status of the pilot lamps.
IL02--LT	Marks the end of a DPU program or that the DPU has started to transfer data to the display register R0.
IL03--LT	Marks that one of the rotaries on the front panel has been turned.
IL04--LT	Is reserved for use by an option.
IL05--LT	Marks the end of a display cycle.
IL06--LT	Not used.
IL07--LT	Marks that the power goes down.

8.6.4 Circuit description

The MICROPROCESSOR (D1717) is connected via the microprocessor data bus to the BIDIRECTIONAL DATA BUS BUFFER and to ROM0 and ROM1. ROM0 and ROM1 consists each of two 128K x 8 ROMs, together forming two 128K x 16 ROMs.

If software releases with 64K x 8 ROMs are used, then the soldering joints J1701 and J1702 should be changed over.

The ROMs are addressed via the microprocessor address bus. This bus is buffered to the other units by the ADDRESS BUS BUFFER.

The circuit consisting of D1737, D1741 and D1747 generate the memory select signals and some strobe signals.

The circuit consisting of D1744 and D1746 generate the I/O select signals. Via D1743 and D1714 DATRAKLT goes down with a short delay as one of the I/O select signals goes down.

DATRAKLT can also be pulled down by circuits on other units via pin C8 on connector X1701 and the service switch X1707. This switch can be changed over to generate a data transfer acknowledge by the SLBUENLT signal, which is used by the diagnostic software (see chapter 11.4.4). The circuit around D1741 generates ROM select signals and some other control signals.

The 3 function control signals are applied to a gate in D1737, which detects the interrupt acknowledge status of the microprocessor, when all function code signals are high. This is used to generate VAPEADLT and memory select control signals.

The monostable multivibrator D1709 keeps the bus busy signal a while active, after the microprocessor has accessed the display RAM. This prevents other microprocessors on options to take over the bus, when the microprocessor has transferred data to the display memory, to assure enough time for the display memory control logic to write the data in the display memory (unit A4).

The BUS ARBITER

The BUS ARBITER consists of a dedicated IC (D1731) and associated logic.

It's main function is to assign control of the microprocessor busses to the microprocessor that claims the control.

When no options are installed in the instrument there is only one microprocessor, so the bus arbiter has no real arbiter function.

If UPAB23 at D1734 pin 13 goes high, then RQCL to the BUS ARBITER goes high. Now the BUS ARBITER circuit makes ABBUENLT and SLBUENLT low, which enables all buffers to the CCU-bus. This enables the microprocessor to access memory and I/O ports on other units via the CCU-bus.

The BUS ARBITER circuit is reset by the microprocessor reset signal (UPRGOTLT) from the RESET/HALT logic.

The capacitors C1754...C1761 and resistor network R1726 give delay times, which time the taking over of the microprocessor busses by another microprocessor.

The associated logic generates a number of control signals for the arbiter function as well as for normal microprocessor functions. The shift register D1748 generates the CLWR--LT signal that lies with its edges between the edges of one of the memory select signals. So first the memory select signal goes down, next the CLWR--LT pulse and UPWR--LT pulse at D1721 come and finally the memory select signal goes high.

The CLOCK GENERATOR consists of a compact integrated crystal oscillator of 16 MHz (G1701) and a number of divider stages. The table below gives the frequency of the generated signals.

Name	Frequency
UPCK16	16 MHz
UPCK08	8 MHz
UPCK	8 MHz
Z-MO-XT	200 kHz
TIC	25 Hz

By changing over soldering joint J1707 all frequencies are divided by 2. This can be used to detect access time problems.

The INTERRUPT PRIORITY LEVEL ENCODER (D1708) encodes 7 offered interrupt levels to a 3 bit binary code (IPL0...2), which is applied to the microprocessor. A reaction of the microprocessor on IL01--LT might be postponed a while, because interrupts with a higher priority are present. Now flipflop D1704 keeps IL01--LT low, when TIC goes high after 20 ms. When the interrupt is acknowledged the flipflop is reset by TCRS--LT.

Gate D1739 is a buffer between the HCT logic on unit A3 and the LS TTL logic of D1708.

IL07--LT (power down) is also routed to the reset/halt logic, to halt the microprocessor.

The WATCHDOG consists of a retriggerable monostable multivibrator (D1709), an oscillator (D1712) and the reset/halt logic.

When the microprocessor program runs normally, the multivibrator is retriggered within every 2 seconds by WD---LT. This keeps pin 12 of D2709 low. Via D1712 UPRSOTLT and UPHA--LT stay high.

When another microprocessor has taken over control over the system, WD---LT is generated by this microprocessor.

If the WD---LT signal does not come within 2 seconds (e.g. due to an abnormal program sequence) pin 12 of D1709 goes high. Now the microprocessor is halted by UPHA--LT and the hardware is reset by UPRSOTLT.

The gate of D1712 pins 1, 2 and 3 forms an oscillator, so after about 2 seconds UPHA--LT and UPRSOTLT become inactive. The microprocessor will restart, generate the WD---LT signal and so on.

If for some reason the microprocessor should not restart correctly the oscillator of D1712 gives a halt plus reset after 2 seconds and after another 2 seconds the microprocessor can restart again. The strap X1708 allows disabling of the watchdog, which is used for the diagnostic software (see section 11.4).

A start of the microprocessor and a restart caused by the watchdog initiates the power up routine (see section 11.4).

If the power goes down IL07--LT halts the microprocessor via pin 5 of D1712. Capacitor C1753 keeps IL07--LT long enough low at power up, to be sure that all supply voltages are present when the microprocessor starts.

The signal IL07--LT is also connected to testpoint X1713, which is located next to ground testpoint X1714.

By interconnecting these testpoints the microprocessor can be restarted.

The INPUT PORT enables the microprocessor to read the status of 3 service switches and the status of the battery.

Service switch X1703 is read by the microprocessor to detect in which type of instrument it is placed, to start up the appropriate software. In this instrument the switch should be open (see figure 8.6.1).

Service switches X1704 and X1706 have functions for the diagnostic software (see section 11.4.4).

Via the OUTPUT PORT, the microprocessor generates the watchdog signal WD---LT with the open collector gate D1714. The battery test circuit is also controlled via the output port.

The BATTERY TEST circuit loads the battery via V1702 and R1712 with a specified current, when the condition of the battery has to be tested after a (re)start of the microprocessor. The COMPARATOR compares the battery voltage with a reference voltage from V1701. When the battery voltage is too low, BAST goes high, which is read by the microprocessor via the input port.

The SUPPLY VOLTAGE SWITCH switches +5D off, when this voltage is too low.

When the power is on, +5D supplies the memories via V1712. V1707 prevents that the batteries are charged by +5D.

When +5D goes too low as the instrument is switched off, V1711 and V1712 block.

Now the memories are supplied by the battery via V1707. The blocking diode V1712 prevents that the battery supplies back to +5D.

V1708 will also block, MYSLDWLT will go down, which will deselect the memories. Their contents will remain.

8.6.5 Signal name list

UNIT A6

Signal name	Description	Signal source	Signal destination(s)
AB01...20	Address bus 01...20	A6+Option	General
ABBUENLT	Address bus enable	A6	A6
BAST	Battery status	A6	A6
BATS	Battery test	A6	A6
BAVO	Battery voltage	A66	-
BSBU--LT	Bus busy	A6+Option	A6,Option
BSGROHT	Bus grant output	A6	Option (1)
BSRQ--LT	Bus request	A6+Option	A6,Option
CLWR--LT	Clocked write	A6	A6
DAAK--LT	Data acknowledge	A6	A6
DAAKBSLT	Data acknowledge bus	A6	A6
DAHISBLT	Data high strobe	A6+Option	A12-A3,A12-A5
DALOSBLT	Data low strobe	A6+Option	A12-A3,A12-A5
DASB--HT	Data strobe	A6	A6
DATRAKLT	Data transfer acknowledge	A3+A5+A6+A8+Option	A6,Option
DB00...15	Data bus 00...15	A6+Option	General
ENAD--LT	Enable address	A6	A6
FC0...2	Function code 0...2	A6	A6
IL01--LT	Interrupt level 01	A6	A6
IL02--LT	Interrupt level 02	A8	-
IL03--LT	Interrupt level 03	A14	-
IL04--LT	Interrupt level 04	Option	-
IL05--LT	Interrupt level 05	A3	-
IL06--LT	Interrupt level 06	A25	-
IL07--LT	Interrupt level 07	A20	-
IPL0...2	Interrupt priority level 0...2	A6	A6
IOSL03LT	I/O Select 03	A6	A12-Option
IOSL04LT	I/O Select 04	A6	A12-A14
IOSL05LT	I/O Select 05	A6	A12-A3
IOSL06LT	I/O Select 06	A6	A12-A25-A26
IOSL07LT	I/O Select 07	A6	A12-A25
IOSL08LT	I/O Select 08	A6	A12-A5
IOSL09LT	I/O Select 09	A6	A12-Option
IOSL10LT	I/O Select 10	A6	A12-Option
LODASBLT	Lower data strobe	A6	A6
MASL--LT	Master selected	A6+Option	A6,Option
MYSL01LT	Memory select 01	A6+Option	A12-A5
MYSL02LT	Memory select 02	A6+Option	A12-A3,A12-A4
MYSL03LT	Memory select 03	A6	A12-A8
MYSL04LT	Memory select 04	A6	A12-Option
MYSLALHT	Memory select all	A6	A6
MYSLALLT	Memory select all	A6	A6
MYSLDWLT	Memory select down	A6	A12-A4,A12-A5,A12-Option
RDRO	Read ROM	A6	A6
RDSB--LT	Read strobe	A6	A6

(1) Becomes BSGRINHT on option.

Signal name	Description	Signal source	Signal destination(s)
RQCL	Request clock	A6	A6
SLBUENLT	Select bus enable	A6	A6
SLRO0	Select ROM 0	A6	A6
SLRO1	Select ROM 1	A6	A6
TCRS--LT	TIC reset	A6	A6
TIC	Timer interrupt clock	A6	A6
TSLMA-LT	Timing slave to master	A6	A6
UPAB01...23	Microprocessor address bus 01...23	A6	A6
UPADSBHT	Microprocessor address strobe	A6	A6
UPADSBLT	Microprocessor address strobe	A6	A6
UPCK	Microprocessor clock	A6	A6
UPCK08	Microprocessor clock 8 MHz	A6	A12-A4, A12-A8, A12-Option A12-A3, A12-A9
UPCK16	Microprocessor clock 16 MHz	A6	A12-A5 A12-A8 A12-A11
UPDASBLT	Upper data strobe	A6	A6
UPDB00...15	Microprocessor data bus 00...15	A6	A6
UPHA--LT	Microprocessor halt	A6	A6
UPIN--HT	Microprocessor input port	A6	A6
UPOT--HT	Microprocessor output port	A6	A6
UPRD--LT	Microprocessor read	A6	General
UPRDWR	Microprocessor read/write	A6	General
UPRSOTLT	Microprocessor reset out	A6	A12-A3, A12-Option, A12-A5-A12-A25
UPWR--LT	Microprocessor write	A6	General
VAPEADLT	Valid peripheral address	A6	A6
VAPESLLT	Valid peripheral select	A6	A6
VBB	Voltage battery backup	A6	A12-A5, A12-Option
WD----LT	Watch dog	A6+Option	A6
WRSB--LT	Write strobe	A6	A6
Z-MO--XT	Z-modulation	A6	A12-A1

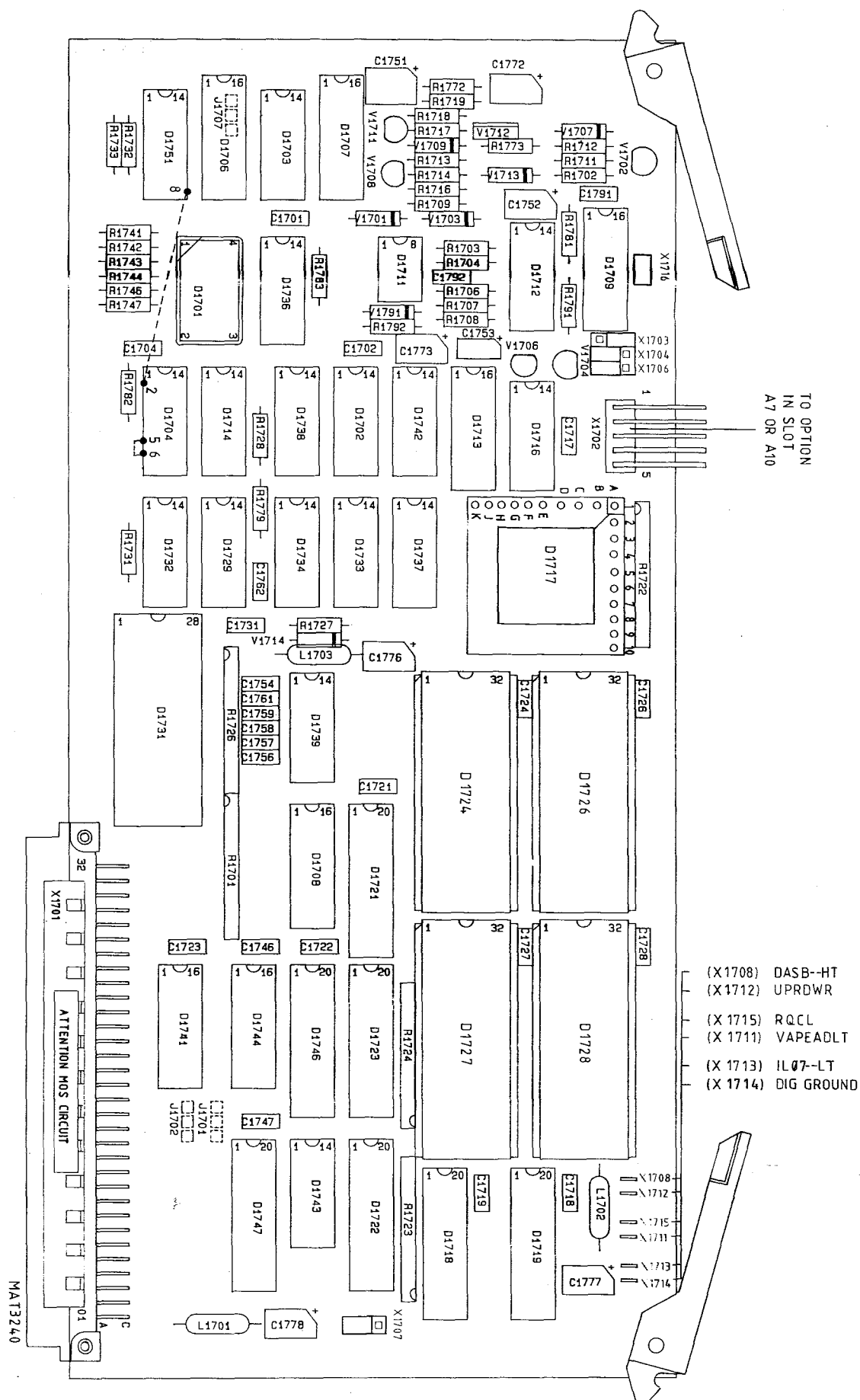
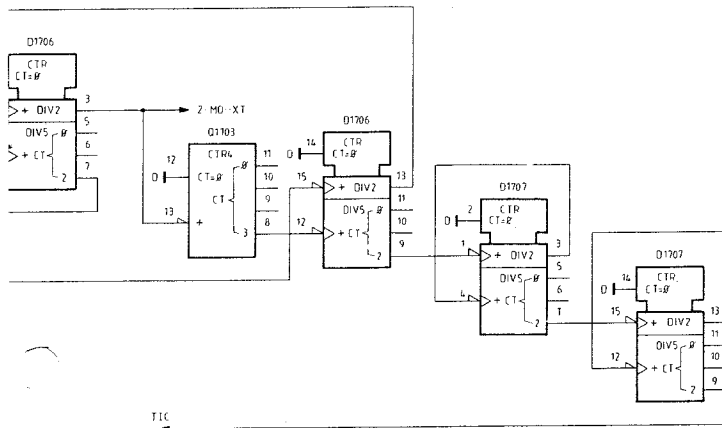
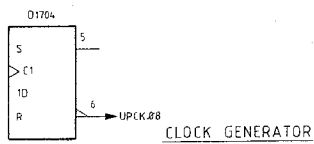
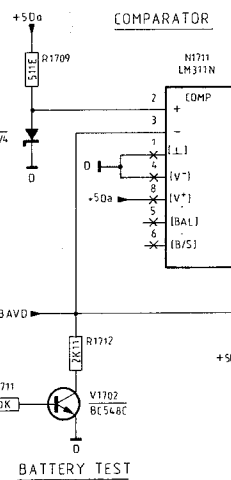
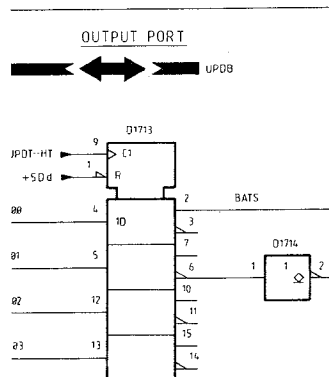
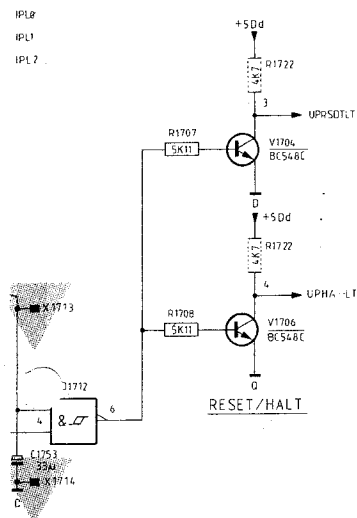


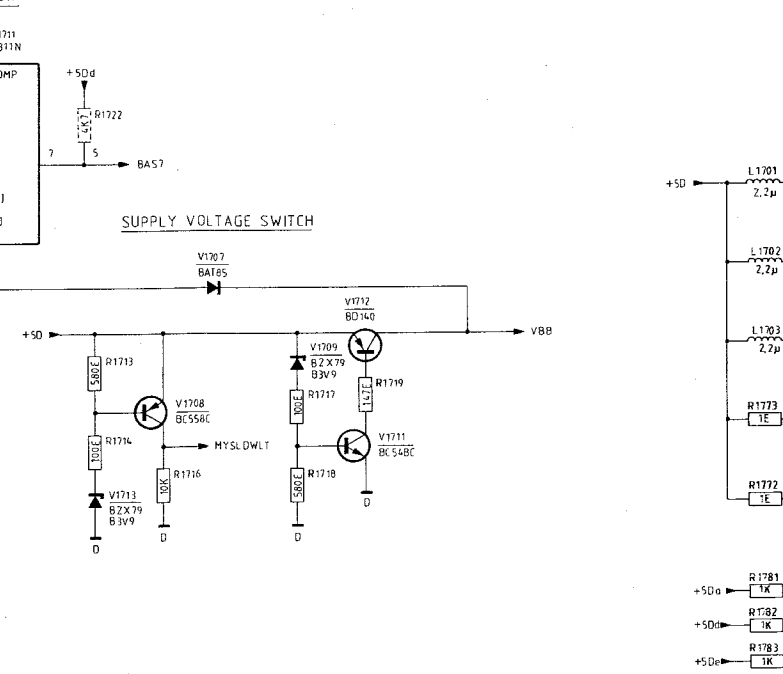
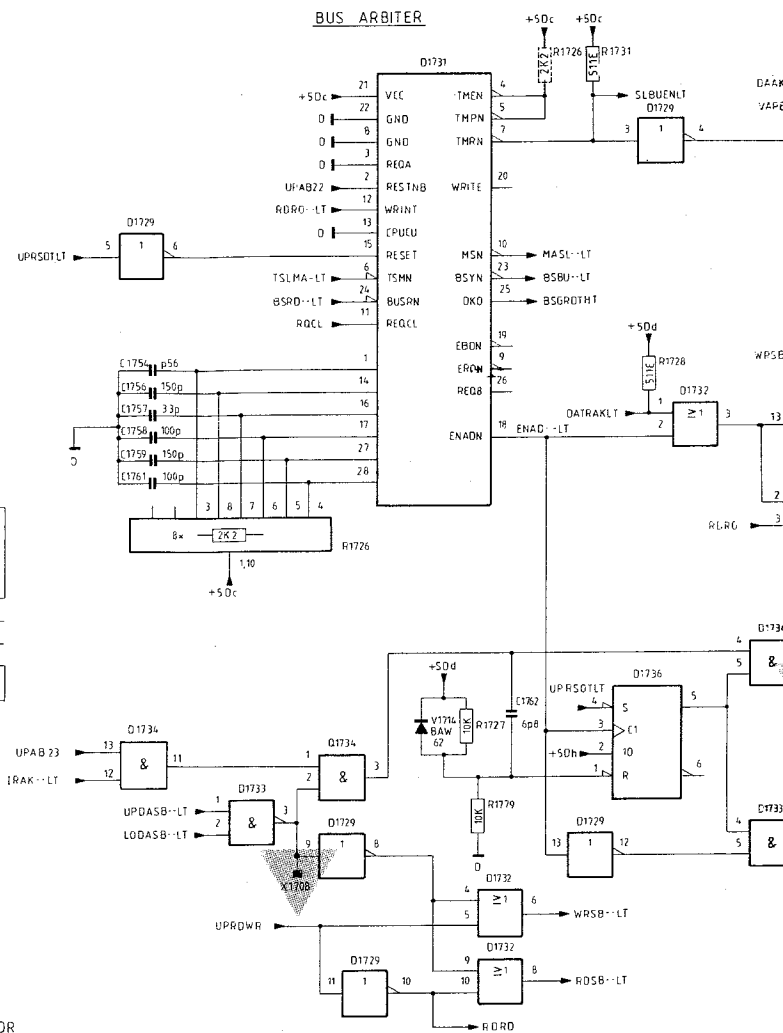
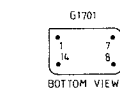
Figure 8.6.1 Unit A6 - UP UNIT - p.c.b. lay-out.



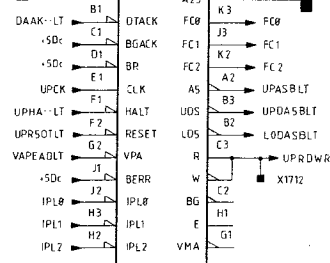
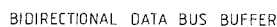
LEVEL ENCODER



BATTERY TEST



circuit diagram.



REFNR	TYPE	VCC AND GND NUMBERS					
		+50A	+50B	+50C	+50B	+50A	+
D1702	74F04				14		7
D1703	74HCT393	14					7
D1704	74F74				14		7
D1706, D1707	74HCT390	16					8
D1708	74LS148					16	8
D1709	74HCT123	16					8
D1712	74HC1132	14					7
D1713	74HC1175				16		8
D1714	74LS05				14		7
D1716	74HC103				14		7
D1717	MC68000REB			02E9			DSE
D1718, D1719			20				10
D1721, D1746, D1747	74LS541	14				20	10
D1722, D1723	74LS245					20	10
D1724, D1726, D1727				1, 30, 31,32			16
D1728	27010						
D1729	74HC104				14		7
D1732, D1738					14		7
D1739	74HC132		14				7
D1733	74HC100				14		7
D1734	74HC106				14		7
D1736	74HC174	14					7
D1737	74HC110				14		7
D1741	74HCT139					16	8
D1742	74HC102				14		7
D1743	74HC130						
D1744	74HC1738					16	8
D1751	74HC1164			14			7

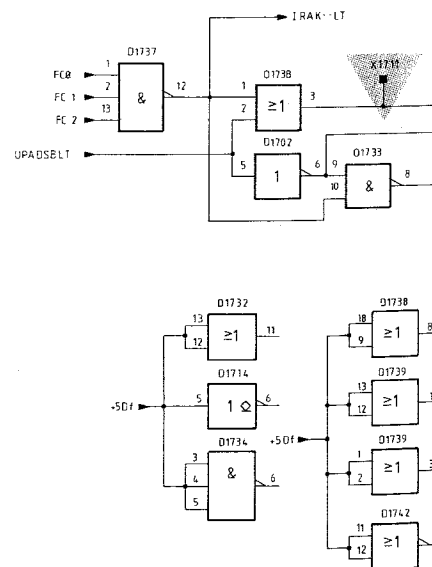
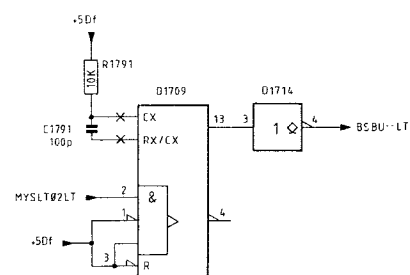
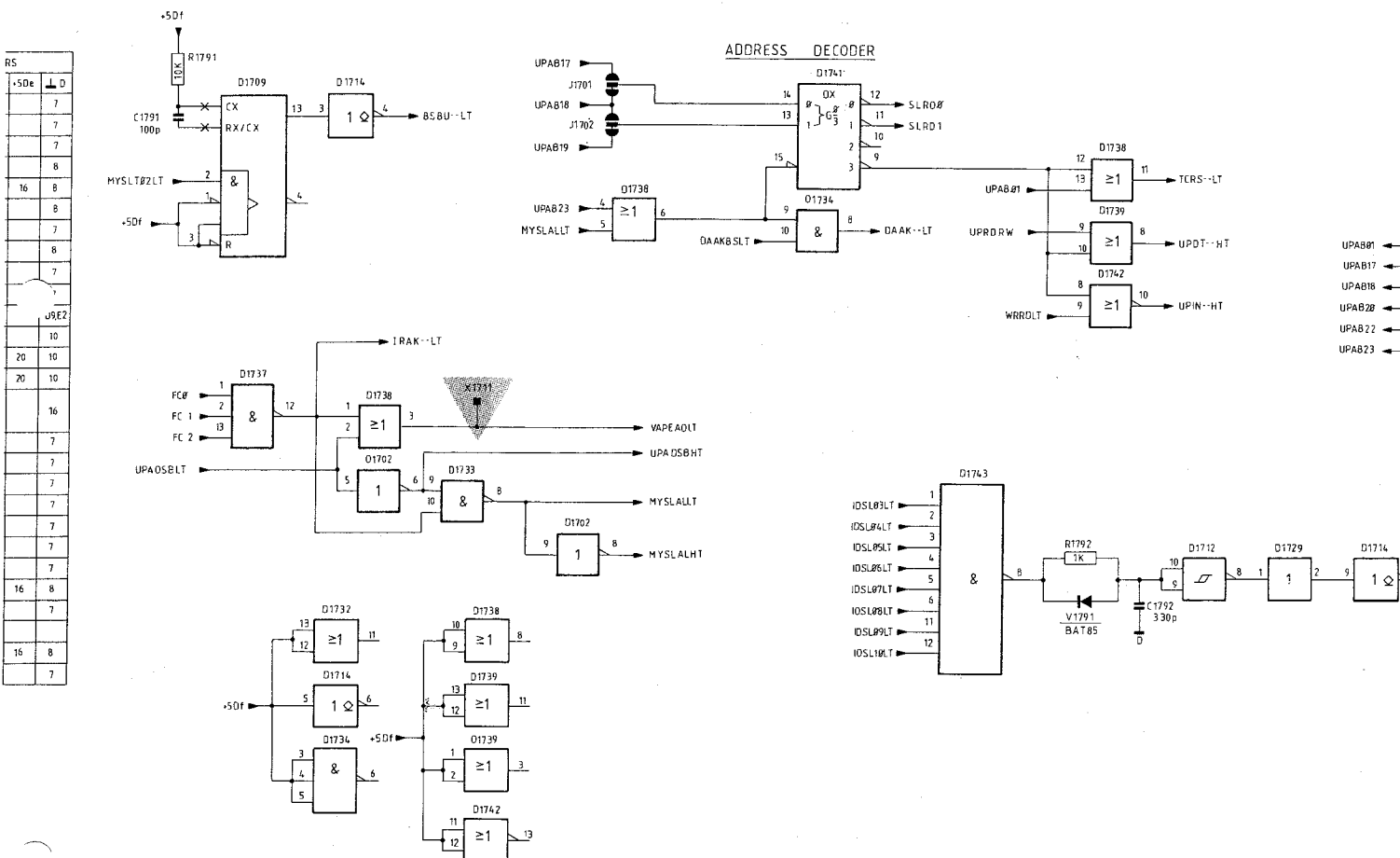
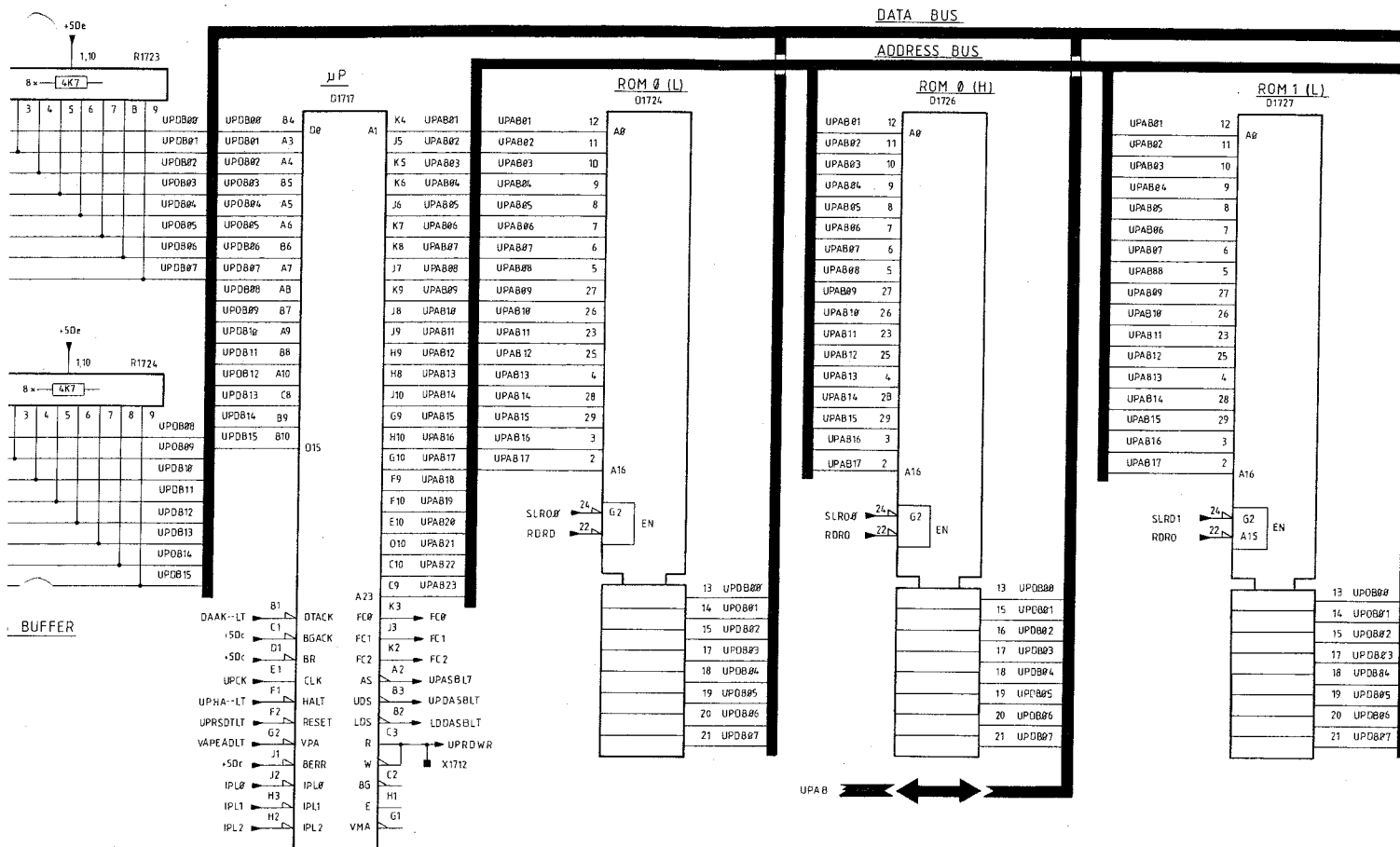


Figure 8.6.3 Unit A6 - UP UNIT - circuit diagram.



P UNIT - circuit diagram.

