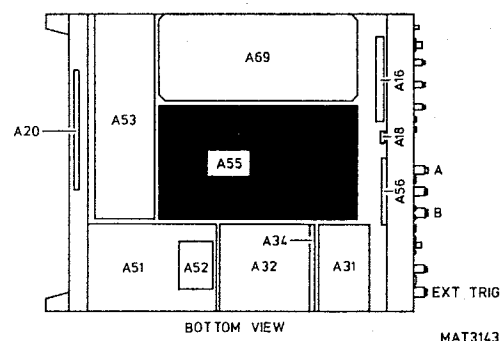


UNIT A55 - VERTICAL SIGNAL UNITCONTENTS

8.55.1	General information.....	8.55-1
8.55.2	Sampling system.....	8.55-1
8.55.3	Circuit description.....	8.55-2
8.55.4	Signal name list.....	8.55-4

## 8.55.1 General information

This unit processes the samples of both channels until they are ready to be accepted by the ADC and T&H unit A11.

Also some auxiliary circuits for the Gate unit are on this unit. Samples on both channels are taken synchronously and processed synchronously until the channel switch on this unit.

## 8.55.2 Sampling system

The sampling system consists for each channel of a SAMPLING GATE on unit A54 and a BRIDGE on unit A55. Figure 8.55.1 shows a simplified diagram of the sampling system of channel A.

Both current sources in the BRIDGE A supply an equal bias current. If the input signal (A), the feedback signal (FBOTA) and the offset signal (OSOTA) are all at ground level, then the system is symmetrical. When sampling pulses occur, the sampling diodes (V907) are in conductance and a part of the bias current of the upper current source will flow through T5001, winding 2-5, R916, R918, V907, R913, R917 and T5001, winding 4-3.

Due to the symmetry, the current through winding 2-5 is equal to the current through winding 4-3. Now the effects of both currents compensate each other, due to the winding sense of both windings. This results in no output voltage from winding 7-8 to the PRE-AMPLIFIER A.

If the input voltage (A) is not equal to zero, then the currents at sample moments through the windings 2-5 and 4-3 will be different, resulting in voltage pulses (samples) from winding 7-8, which are proportional to the input voltage.

If the signals FBOTA and OSOTA are not zero, then the voltages of the BRIDGE A will shift up and down with them. This causes different currents through the windings 2-5 and 3-4 at sample moments, which on their turn result in sample voltages from winding 7-8, which are proportional to FBOTA and OSOTA.

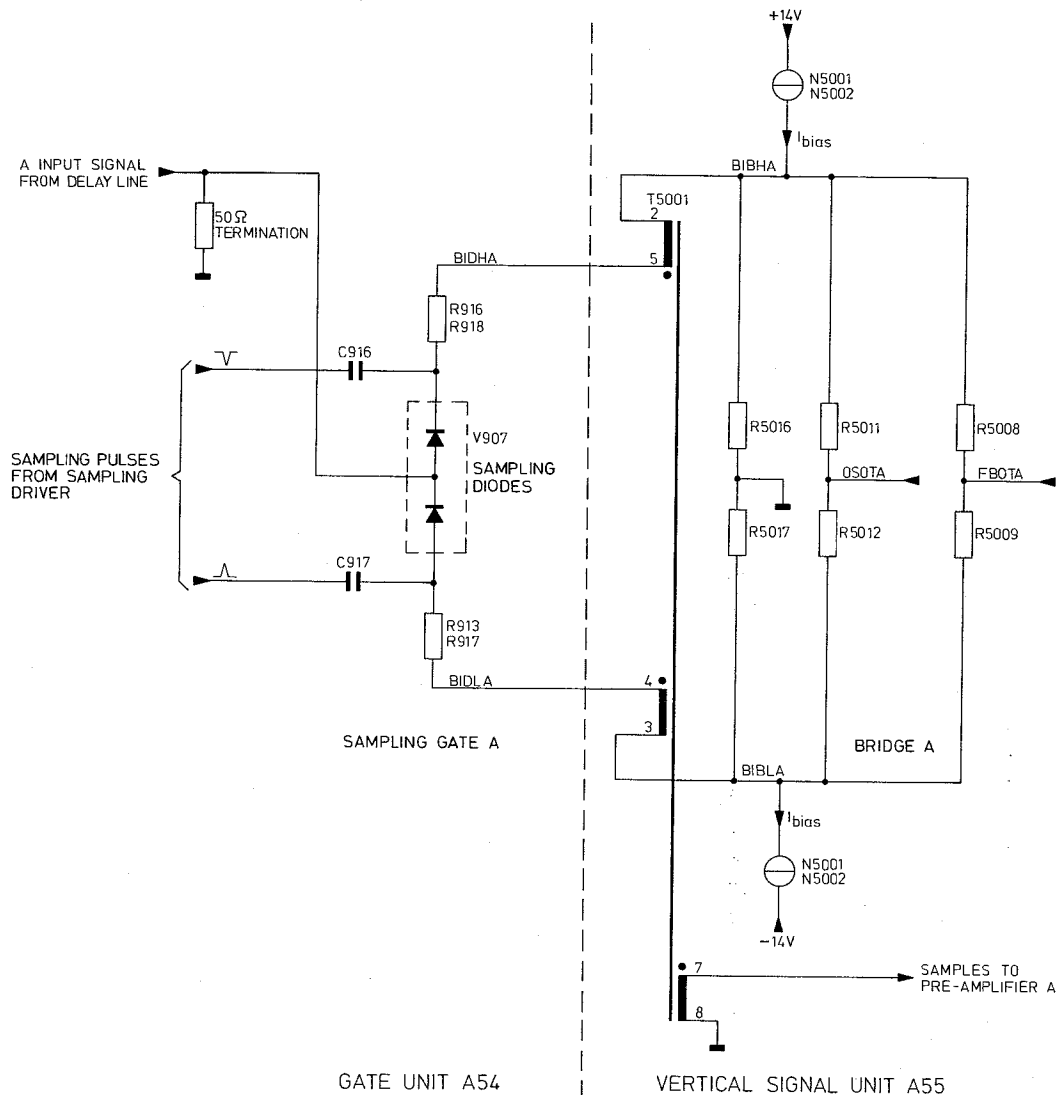


Figure 8.55.1 Sampling system.

### 8.55.3 Circuit description

As both channels are identical only channel A is described.

The BRIDGE A consists of 2 current sources, a resistor network (R5008...R5017) and pulse transformer T5001.

The 2 current sources consist of opamp N5001 and transistor array N5002. The upper current source supplies the bias current for the bridge via pin 15 of N5002. Via a current-mirror circuit, consisting of the remaining transistors of N5002, an equal current is sunk from the bridge via pin 9.

The OFFSET A circuit consists of a number of opamp circuits, which add the offset coarse (OSCRA) and the offset fine (OSFIA) signals. The output signal OSOTA is applied to the BRIDGE A.

The slide switches S5002A...S5003B are used for adjustment purposes.

The analogue feedback signal VBOTA from the Management unit A25 is attenuated by the circuitry around opamp N5004, depending on the selected vertical input sensitivity. The attenuation factor is controlled by the microprocessor. The output signal FBOTA is applied to the BRIDGE A.

The samples from winding 7-8 of transformer T5001 are applied to the PRE-AMPLIFIER A. On a number of nodes an LF-compensation signal (LFCOA) from the Gate unit is applied. Next the amplified samples (PAOTA) are applied to the AMPLIFIER A. The amplification factor is microprocessor controlled and depends on the selected vertical input sensitivity. Next the samples are applied to the TRACK&HOLD A circuit around IC N5006, where they are held on the top of the sample voltage, which enables the ADC on unit A11 to convert the samples of both channels behind each other. The T&H is controlled by the A.C.L. on unit A5 via the T&H SWITCH.

The VERTICAL LATCH is a shift register, which holds the amplification factors and the attenuation factors. It gets its data from the microprocessor via the Management unit A25.

The samples from the TRACK&HOLD A are applied to a multiplying DAC (N5013) in the VARIABLE A circuit. The digital code to the DAC comes from a shift register (D5002), which gets its data from the microprocessor via the Management unit. The output current of the DAC (pin 1) is converted to a voltage by opamp N5014. Next this voltage is applied to the CHANNEL SWITCH, which switches between samples of both channels.

The samples at the output (THINAN) are applied to T&H and ADC unit A11, where they are converted into digital codes.

Furtheron, the unit contains three circuits, which are common for both channels.

The AVALANCHE VOLTAGE circuit is a stabilised voltage supply which supplies the avalanche voltage for the Gate unit.

The SNAP-OFF CURRENT circuit is a current source, which supplies the snap-off current for the Gate unit.

The T&H SWITCH is a buffer between the HDSA-1 signal from the A.C.L. on unit A5 and the T&H circuits on this unit.

The hold moments for both channels can be adjusted separately with R7011 and R016.

This circuit is mounted on an add-on p.c.b. which is fitted on socket X7007.

- Notes:
- As the Vertical Signal unit has a feedback loop, the accuracy of the gain factors is determined by the accuracy of the attenuation factors of the feedback loop.
  - Looking at the bottom side of the oscilloscope, when it is standing on its rear feet, the A-input connector is at the left side of the B-input connector. However on the p.c.b. the right half is used for channel A and the left half for channel B. This is caused by the equal lengths of the delay lines.

## 8.55.4 Signal name list

## UNIT A55

Signal name	Description	Signal source	Signal destination(s)
AM2A	Amplifier x2 A	A55	A55
AM2B	Amplifier x2 B	A55	A55
AM4A	Amplifier x4 A	A55	A55
AM4B	Amplifier x4 B	A55	A55
AM10A	Amplifier x10 A	A55	A55
AM10B	Amplifier x10 B	A55	A55
AT1A	Attenuation x1 A	A55	A55
AT1B	Attenuation x1 B	A55	A55
AT2A	Attenuation x2 A	A55	A55
AT2B	Attenuation x2 B	A55	A55
AT4A	Attenuation x4 A	A55	A55
AT4B	Attenuation x4 B	A55	A55
AT10A	Attenuation x10 A	A55	A55
AT10B	Attenuation x10 B	A55	A55
AT100A	Attenuation x100 A	A55	A55
AT100B	Attenuation x100 B	A55	A55
AVVO	Avalanche voltage	A55	A54
BIBHA	Bias bridge high A	A55	A55
BIBHB	Bias bridge high B	A55	A55
BIBLA	Bias bridge low A	A55	A55
BIBLB	Bias bridge low B	A55	A55
BIDHA	Bias diode high A	A54	-
BIDHB	Bias diode high B	A54	-
BIDLA	Bias diode low A	A54	-
BIDLB	Bias diode low B	A54	-
CHSW-1	Channel switch 1	A25	-
FBOTA	Feedback output A	A25	-
FBOTB	Feedback output B	A25	-
HDSA-1	Hold sample 1	A5	-
LEVEA	Latch enable vertical A	A25	-
LEVEB	Latch enable vertical B	A25	-
LEVGFA	Latch enable variable gain forward A	A25	-
LEVGBF	Latch enable variable gain forward B	A25	-
LFCOA	LF compensation A	A54	-
LFCOB	LF compensation B	A54	-
OSCRA	Offset course A	A25	-
OSCRB	Offset course B	A25	-
OSFIA	Offset fine A	A25	-
OSFIB	Offset fine B	A25	-
OSOTA	Offset output A	A25	-
OSOTB	Offset output B	A25	-
PAOTA	Pre-amplifier out A	A55	A55
PAOTB	Pre-amplifier out B	A55	A55
PRIF-A	Probe information A	A57	-
PRIF-B	Probe information B	A57	-
PRIFA-XA	Probe information A	A55	A53-A25
PRIFA-XB	Probe information B	A55	A53-A25

Signal name	Description	Signal source	Signal destination(s)
SOCUA	Snap off current A	A55	A54
SOCUB	Snap off current B	A55	A54
STSAGT	Start sample gate	A52	-
THINA	Track & Hold input A	A55	A55
THINAN	Track & Hold in analogue	A55	A11
THINB	Track & Hold input B	A55	A55
THMOA	Track & Hold mode A	A55	A55
THMOB	Track & Hold mode B	A55	A55
THOTA	Track & Hold output A	A55	A55
THOTB	Track & Hold output B	A55	A55
SECK1	Serial clock 1	A25	-
SECK2	Serial clock 2	A25	-
SEDA1	Serial data 1	A25	-
SEDA2	Serial data 2	A25	-
VBOTA	Variable backward output A	A25	-
VBOTB	Variable backward output B	A25	-
VFOTA	Variable forward output A	A55	A55
VFOTB	Variable forward output B	A55	A55

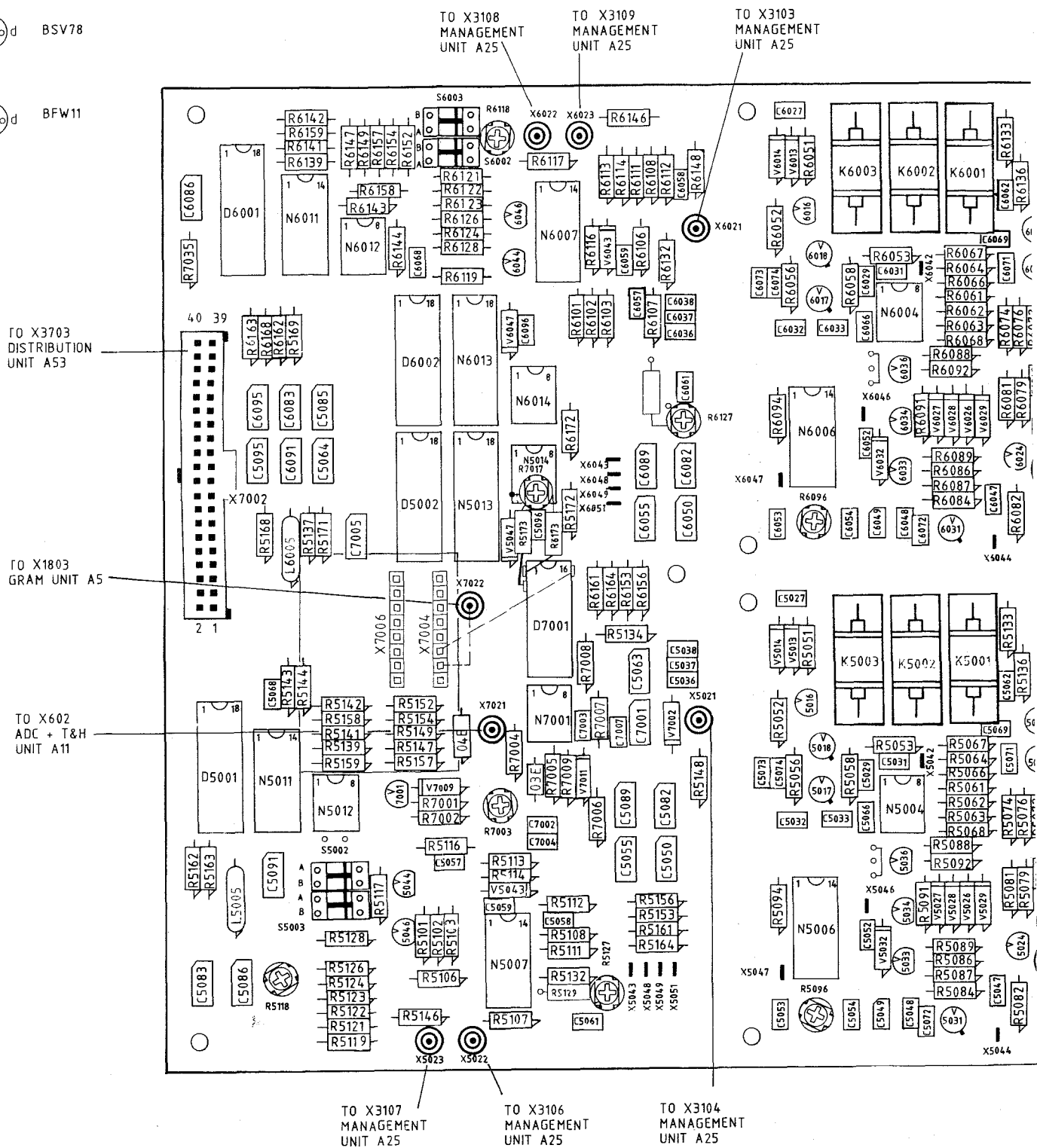
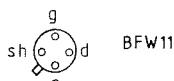
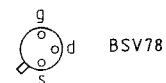
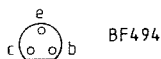
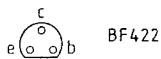
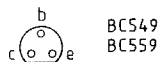
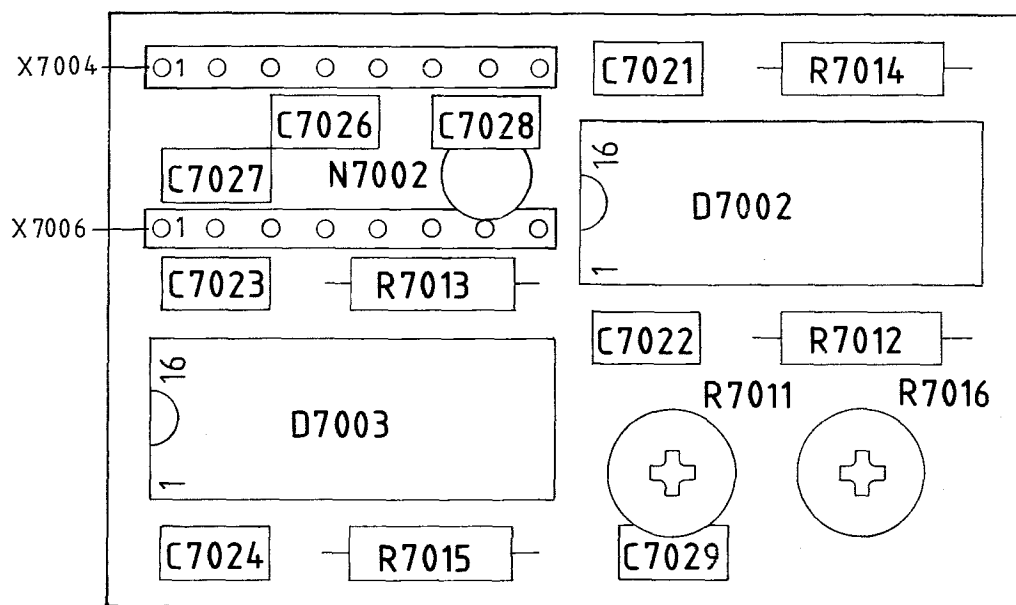
TRANSISTORS  
TOP VIEW

Figure 8.55.2 Unit A55 - VERTICAL SIGNAL UNIT - p.c.b. lay-out.



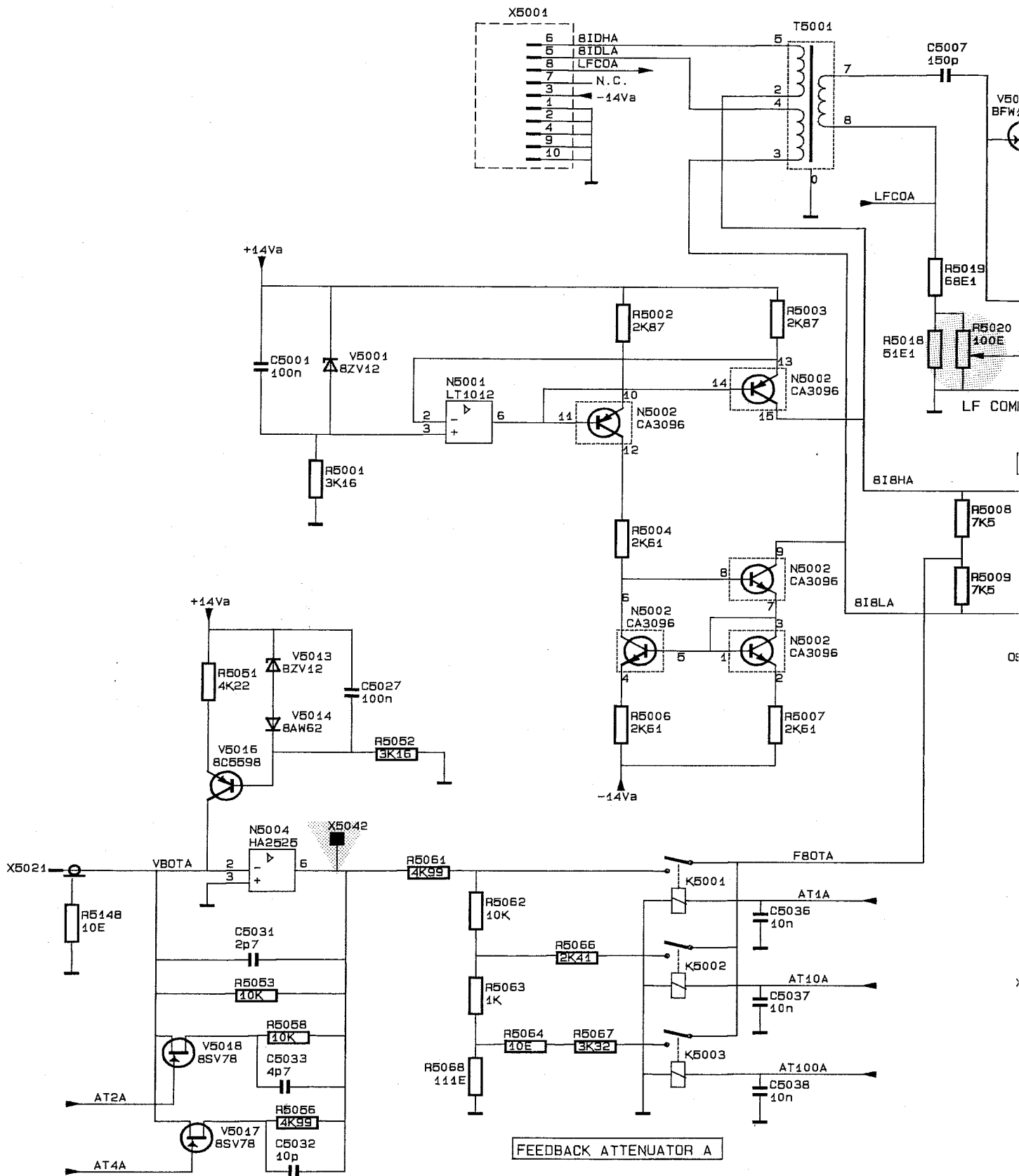


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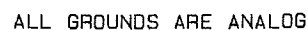
Figure 8.55.3 Unit A55 - VERTICAL SIGNAL UNIT  
P.c.b. lay-out of add-on p.c.b.

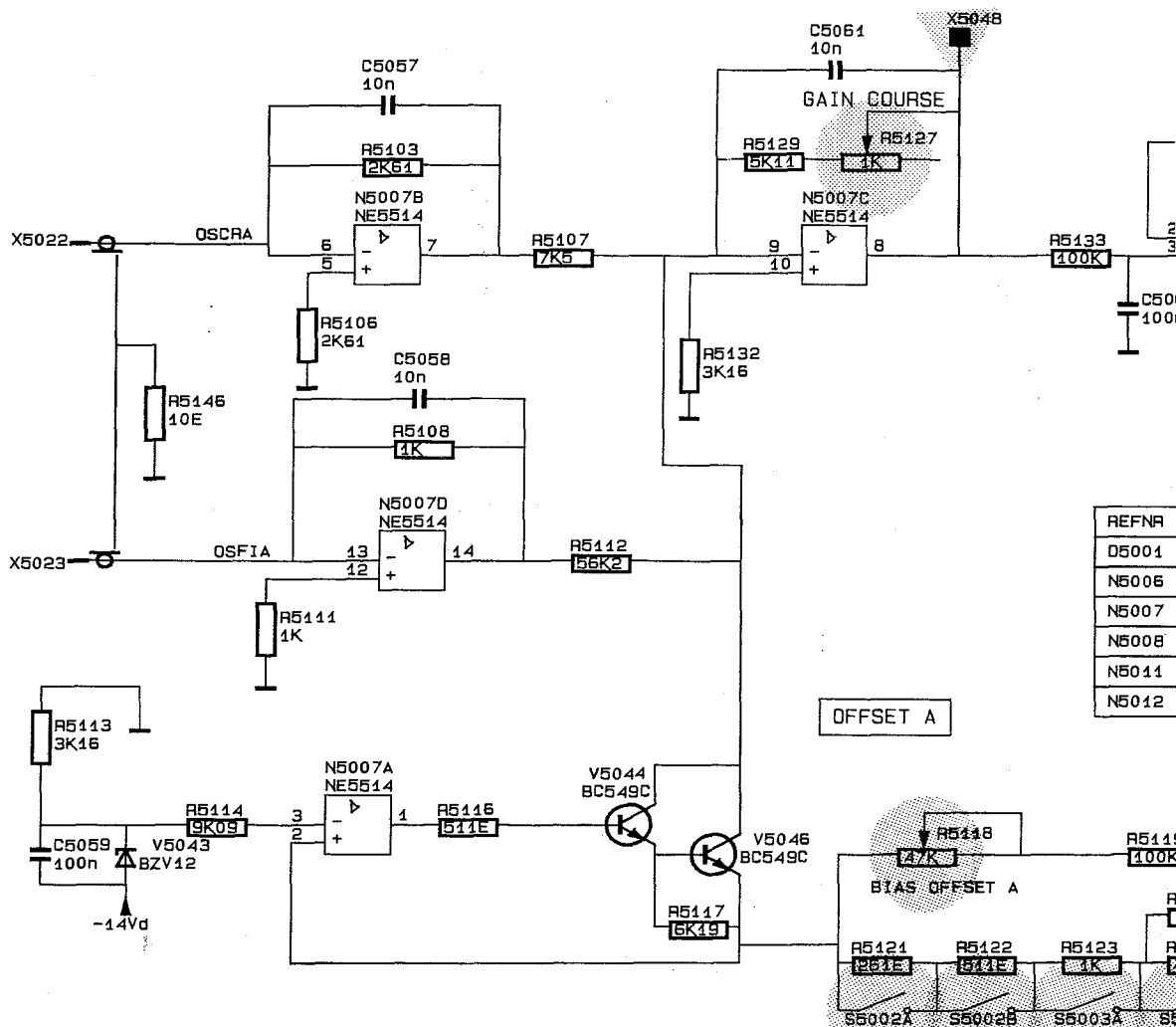
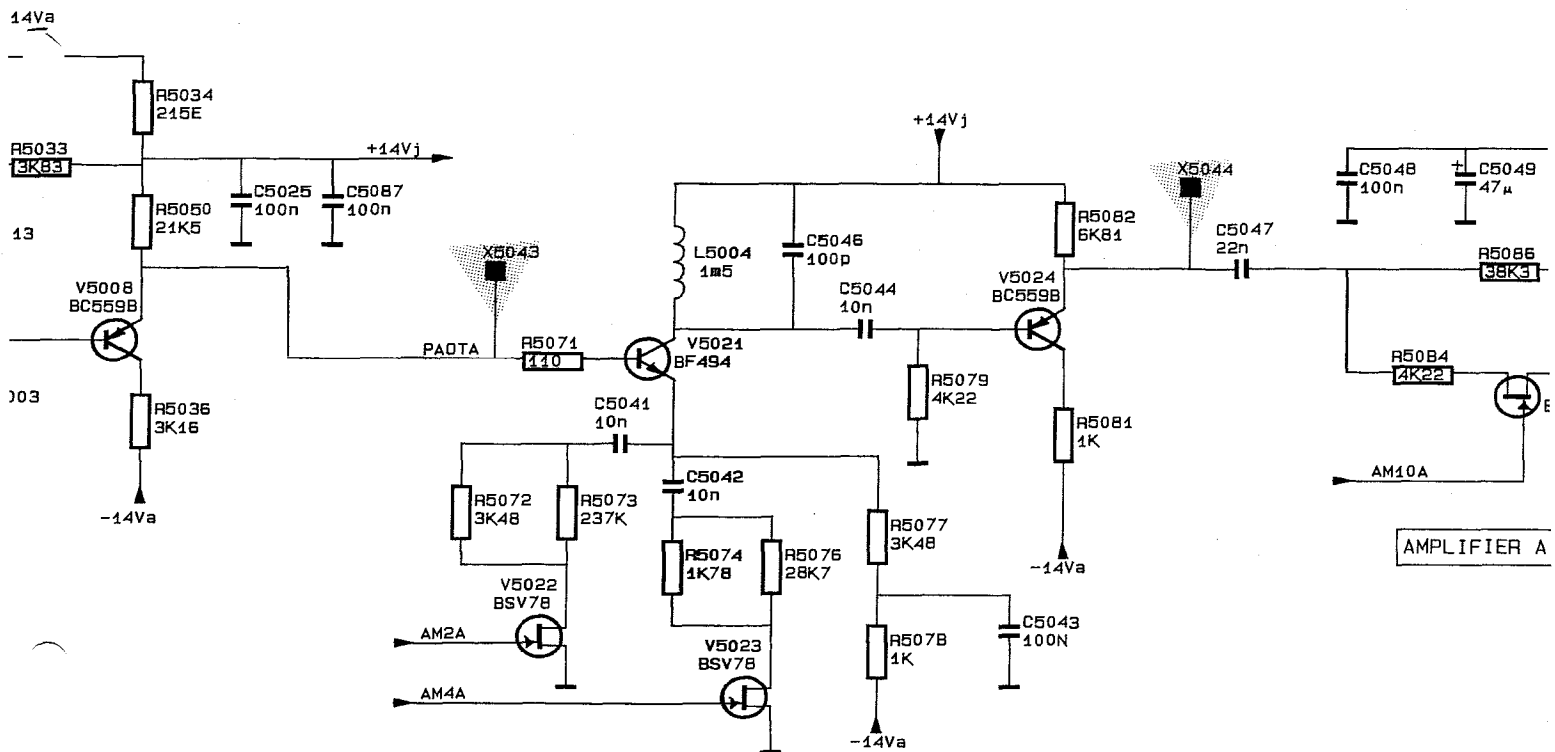


# PRE-AMPLIFIER A



ALL GROUNDS ARE ANALOG





TYPE	+14Va	-14Va	⊥
LT1012	7	4	
CA3096		16	
HA2525	7	4	

REFNR
D5001
N5006
N5007
N5008
N5011
N5012

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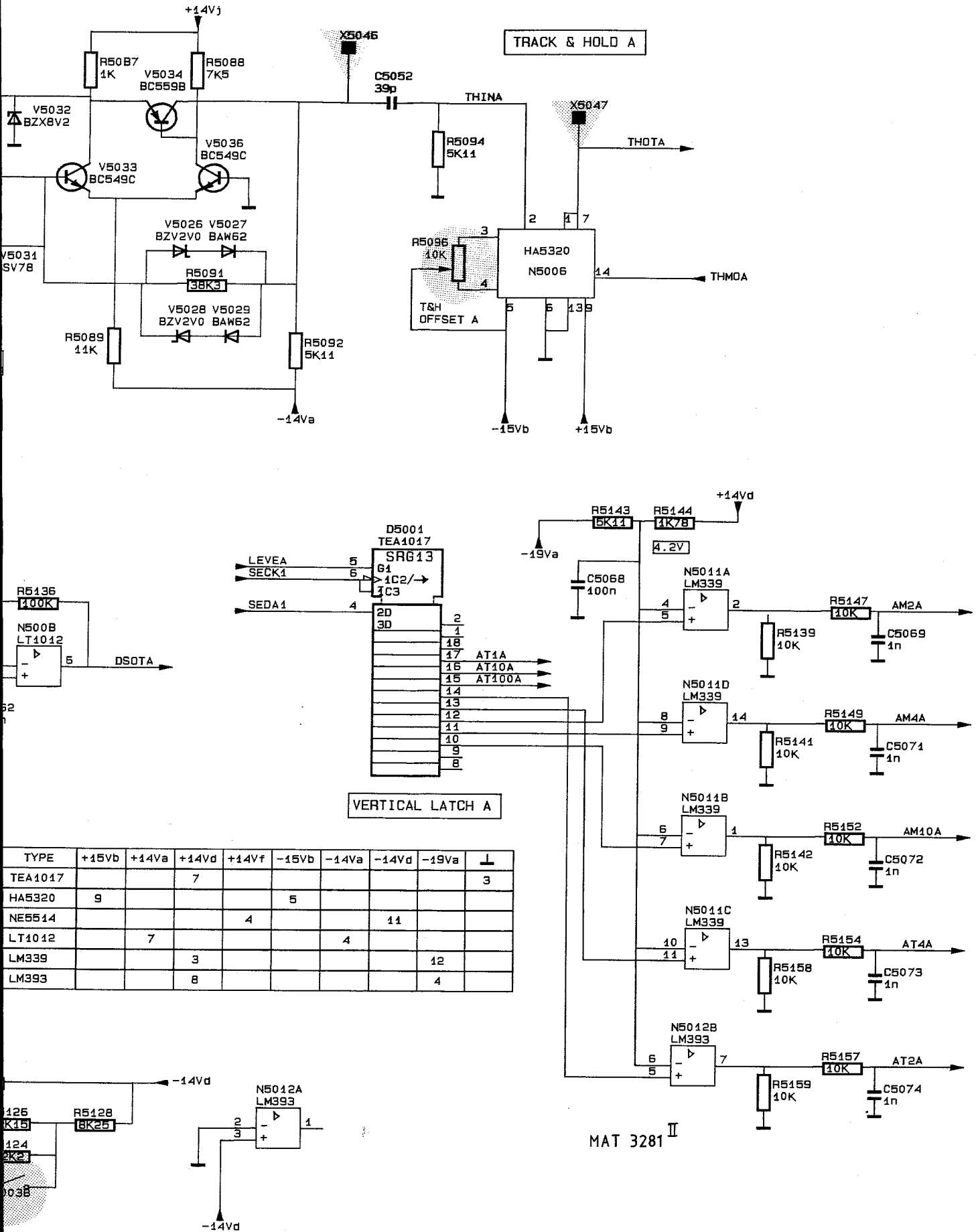
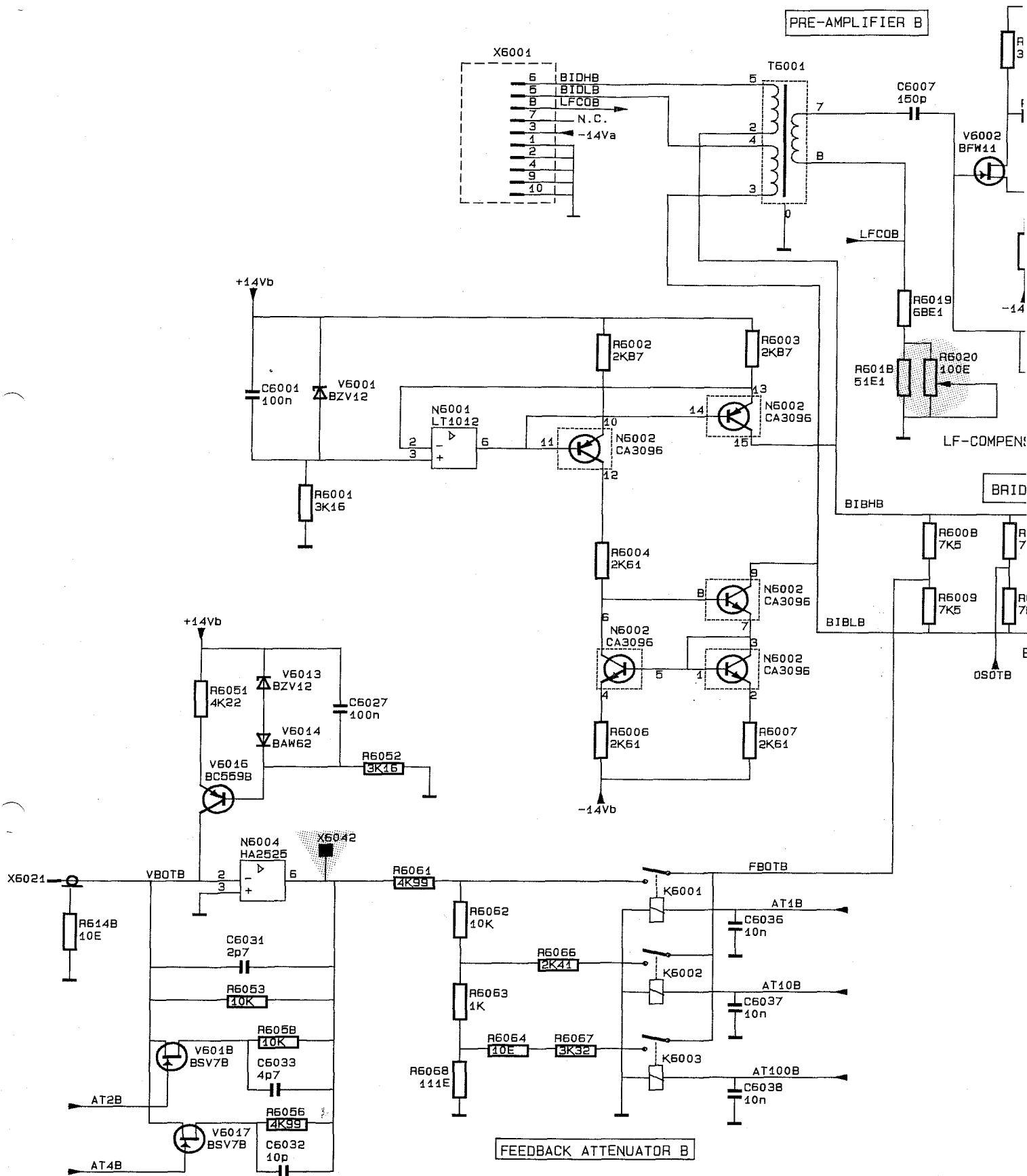
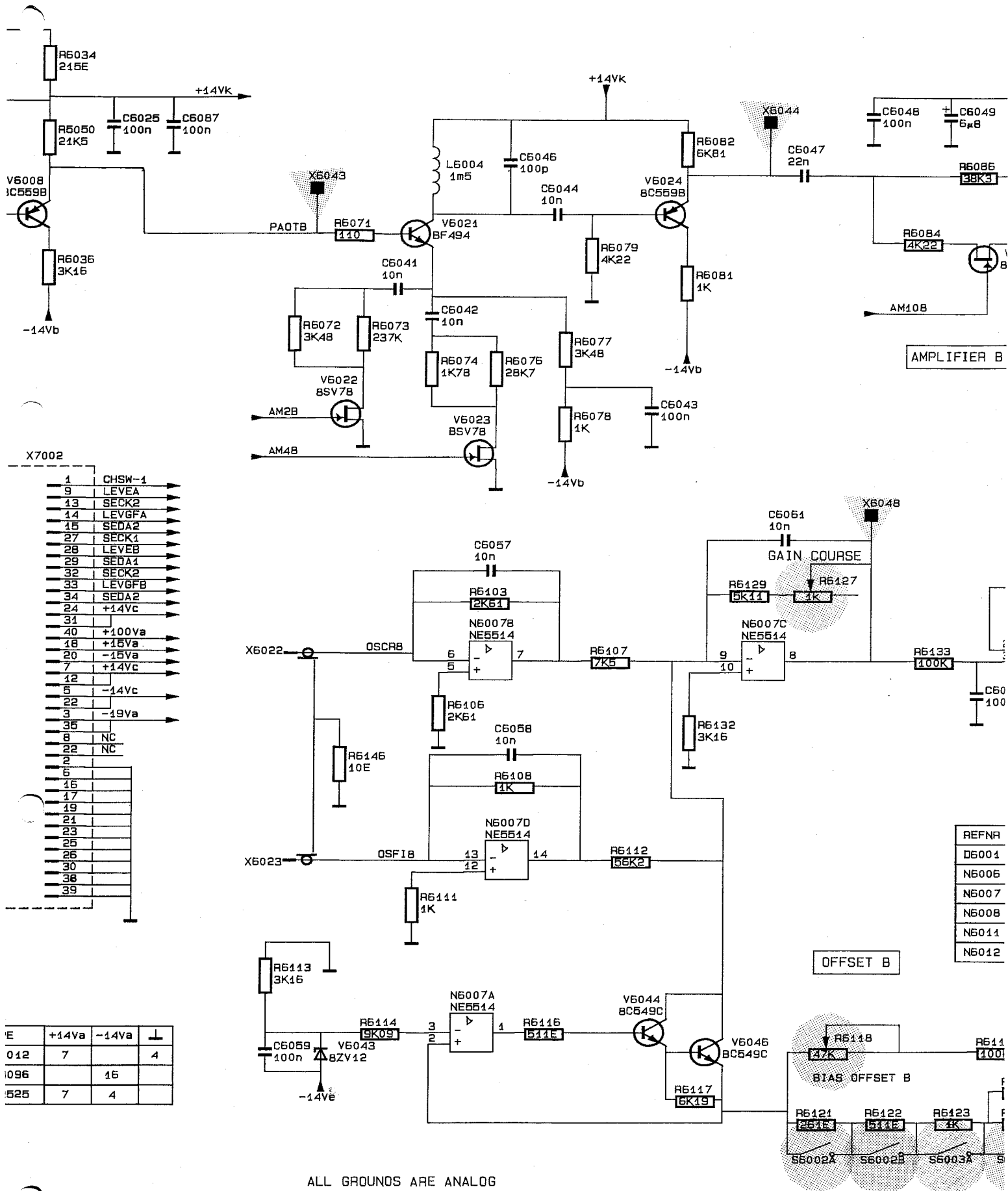


Figure 8.55.4 Unit A55 - VERTICAL SIGNAL UNIT - Circuit diagram.







X7002

1	CHSW-1
9	LEVEA
13	SECK2
14	LEVGF A
15	SEDA2
27	SECK1
28	LEVEB
29	SEDA1
32	SECK2
33	LEVGF B
34	SEDA2
24	+14Vc
31	
40	+100Va
18	+15Va
20	-15Va
7	+14Vc
12	
5	-14Vc
22	
3	-19Va
35	
8	NC
22	NC
2	
6	
16	
17	
19	
21	
23	
25	
26	
30	
38	
39	

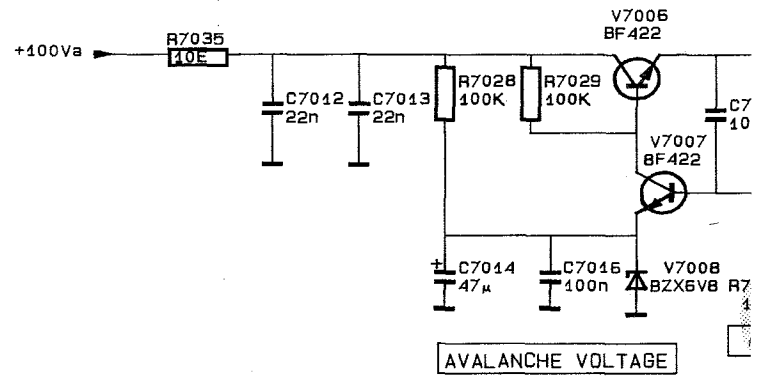
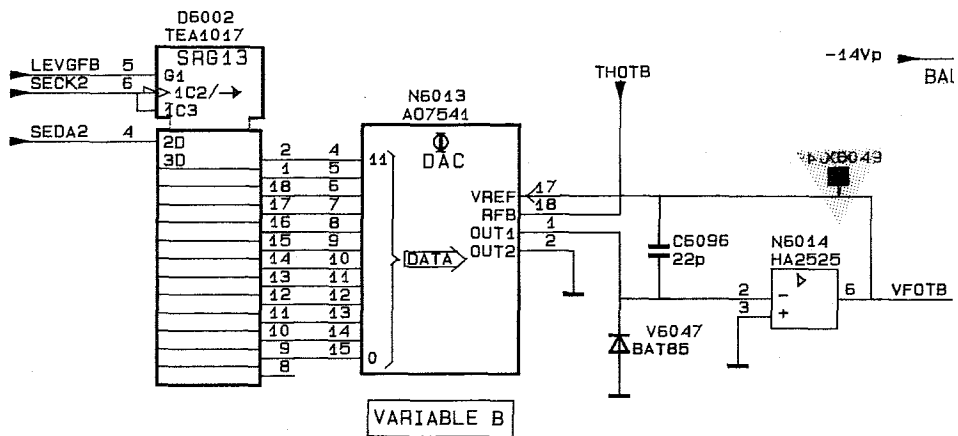
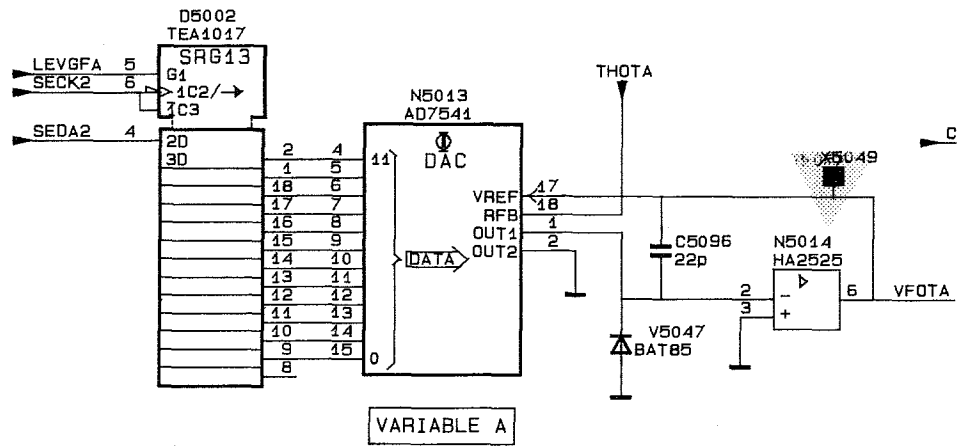
E	+14Va	-14Va	⊥
012	7		4
096		16	
525	7	4	

REFNR

D6001
N6006
N6007
N6008
N6011
N6012

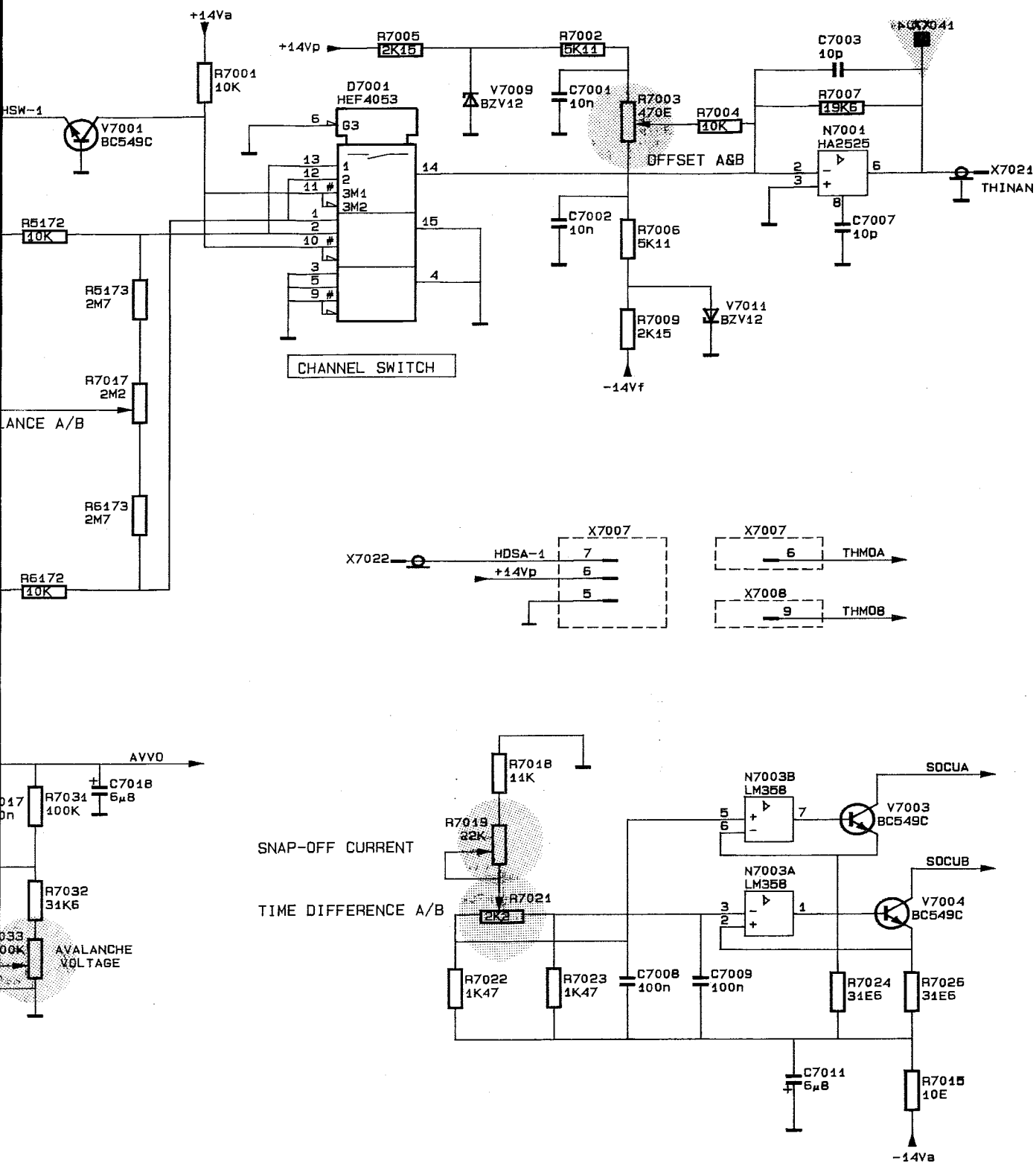




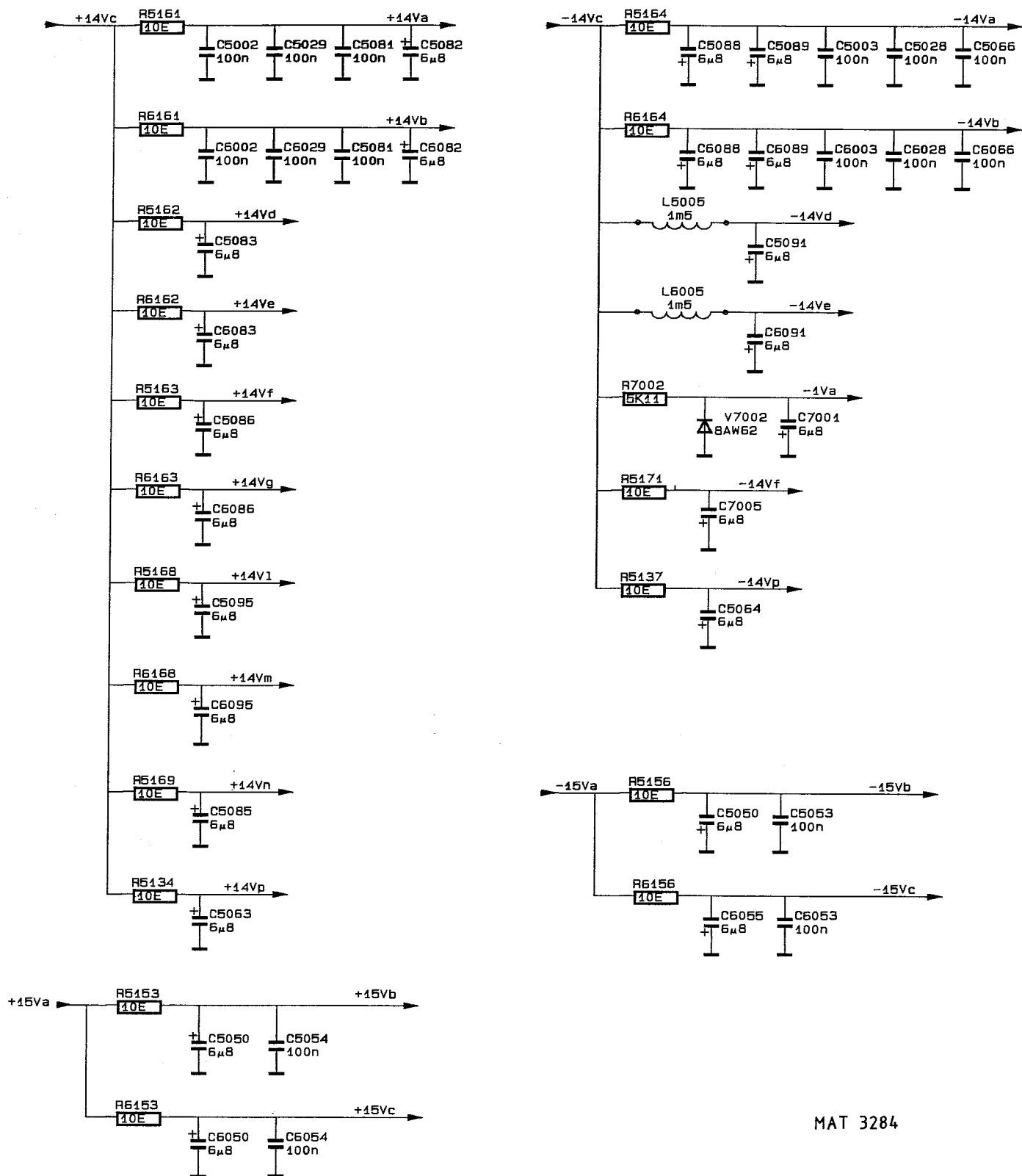


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Figure 8.55.6 Unit A55 - VERTICAL SIGNAL UNIT - Circuit diagram



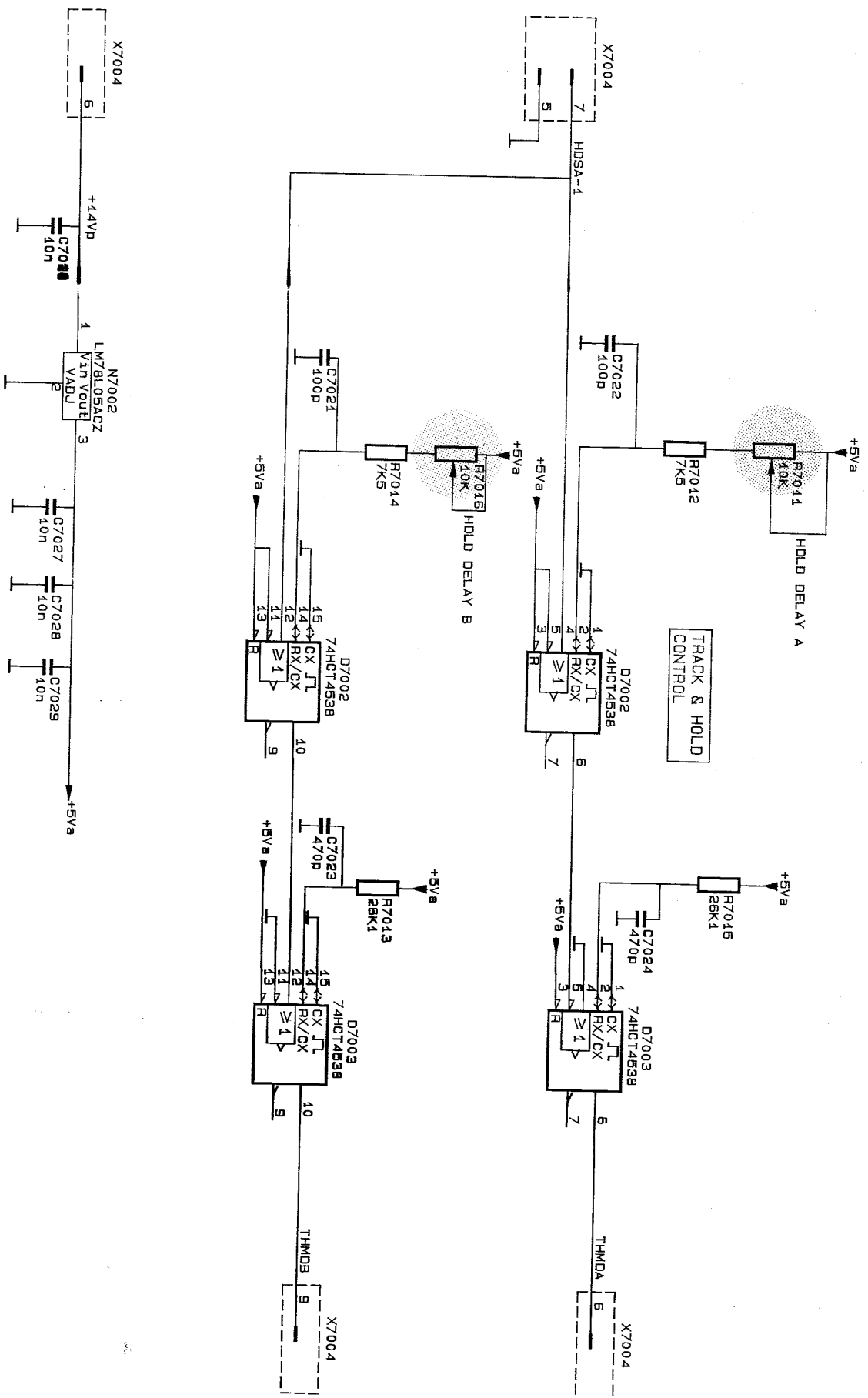
MAT 3283



MAT 3284

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Figure 8.55.7 Unit A55 - VERTICAL SIGNAL UNIT - Circuit diagram.



REF. NR	+5V <sub>a</sub>	1
D7002	16	A
D7003	16	B

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Figure 8.55.8 Unit A55 - VERTICAL SIGNAL UNIT  
Circuit Diagram of add-on p.c.b.