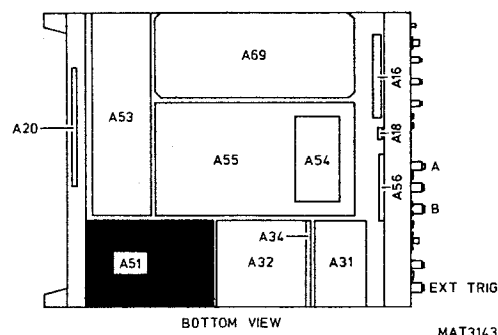


UNIT A51 - TIME-BASE UNITCONTENTS

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8.51.1 General information

In this section the Fast Ramp unit A52 is also described. The main function of the Time-base unit and the Fast Ramp unit is the generation of sampling pulses for the Gate unit. The TRIGGER DELAY function and the HOLD OFF function are also performed on these units. The Fast Ramp unit A52 is built up with S.M.D. technology.

8.51.2 Functional description

Figure 8.51.1 gives a simplified block diagram of units A51 and A52 and their environment.

At the start of a scan the STAIR COUNTER is reset, so the output voltages of the STAIR DAC and the STAIR ATTENUATOR are 0 Volt.

If no trigger delay is selected, the output voltage of the TRIGGER DELAY DAC is 0 volt. So the staircase voltage behind the ADD INVERT circuit (STOT--XA) is 8 volt, because -8 Volt is added.

The TRIGGER DELAY DAC, the STAIR COUNTER, the STAIR DAC, the STAIR ATTENUATOR and the ADD INVERT circuit form the stair generator.

The start level of the FAST RAMP GENERATOR is 8 volt (FSRMOT--XA).

After a trigger this voltage goes down. Now the FAST RAMP/STAIR COMPARATOR will generate immediately a sampling pulse to the SAMPLING GATES on unit A54 and to the ACQUISITION CONTROL LOGIC (A.C.L.) on unit A5.

The A.C.L. gives on its turn a count pulse to the STAIR COUNTER to increase the staircase voltage with 8 mV.

Meanwhile the output voltage of the fast ramp generator crosses the final level, which results in a signal from the END OF FAST RAMP COMPARATOR to the HOLD OFF TIMER. Also the FAST RAMP GENERATOR is reset to 8 volt. Because the stroke of the fast ramp is constant, the total hold off time remains constant.

The HOLD OFF TIMER blocks trigger pulses via the Three Stage Trigger unit A32. When the hold off time is passed the trigger pulses are released again and the next incoming trigger pulse will start the fast ramp.

Now the sampling pulse comes later because the stair case voltage is lower than 8 volt. Therefore the sample is taken a while later on the input signal.

When 512 samples are taken the scan is complete and the A.C.L. is reset by the DPU. Next the A.C.L. resets the STAIR COUNTER. Now the output voltage of the stair generator, which was arrived at about 4 volt, is set to zero.

Other time-base settings are realised by adapting the steepness of the fast ramp.

Because the stair generator covers a range of 4 volt only half the fast ramp voltage range is used.

To obtain a trigger delay, the TRIGGER DELAY DAC gives for example a voltage of 4 volt, which results in a stair case voltage of 4 volts at the start of a scan. Because the fast ramp starts at 8 volts, a trigger delay of 10 divisions is obtained.

To obtain longer trigger delays, the output voltage of the STAIR DAC is attenuated by the STAIR ATTENUATOR and the steepness of the fast ramp voltage is decreased.

8.51.3 Fast ramp generator

Figure 8.51.2 shows a simplified diagram of the FAST RAMP GENERATOR.

The FAST RAMP GENERATOR is built around the time-base capacitors C3504 and C3506.

It consists of three current sources, which are in a closed loop.

The fast ramp current from transistor V3324 on unit A51 is led into the resistors R3361 and R3362. The resulting voltage controls two current sources, one around opamp N3317 and one around opamp N3318. Because R3361, R3362, R3364, R3366 and R3371 have all the same value, the transistor V3509 sinks 4x the fast ramp current and V3327 sinks 2x the fast ramp current.

The latter current is doubled in a similar way as just described by the current source around opamp N3319, because R3372, R3373 and R3374 have the same value. So transistor V3506 supplies 4x the fast ramp current.

To stabilise the loop, a set current is sunked by a current source around transistor V3328. Transistor V3513 will sink 2x this set current to achieve a stable situation.

The balanced pair transistors V3513 and V3514 will make the voltages on their bases equal. The voltage on the base of V3513 is equal to the voltage on the time-base capacitors C3504 and C3506 via the buffer consisting of FET V3512 and transistor V3505. In this way the start level of the time-base capacitors is controlled by potentiometer R3384.

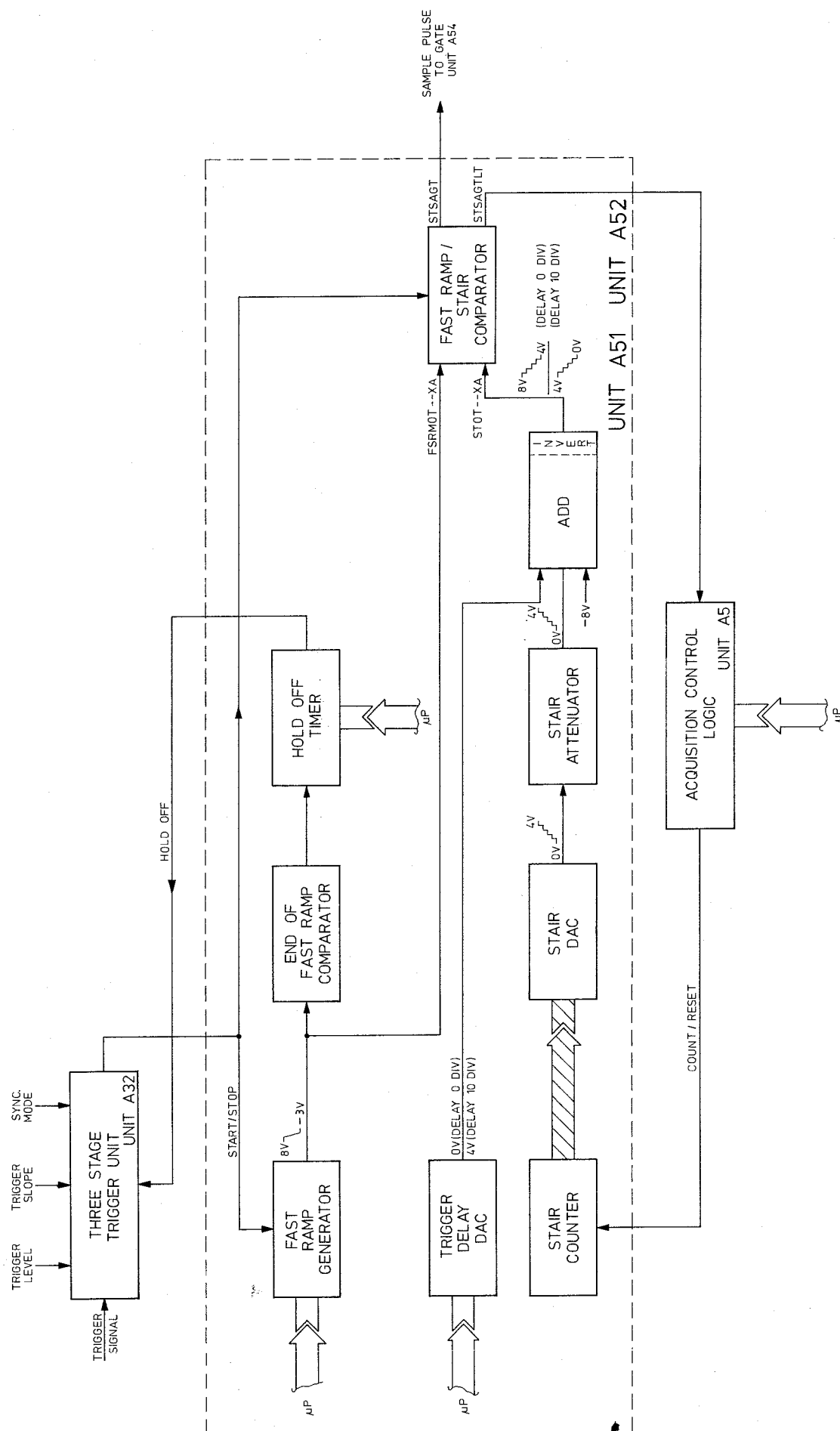


Figure 8.51.1 Block diagram of Time-base unit and Fast Ramp unit.

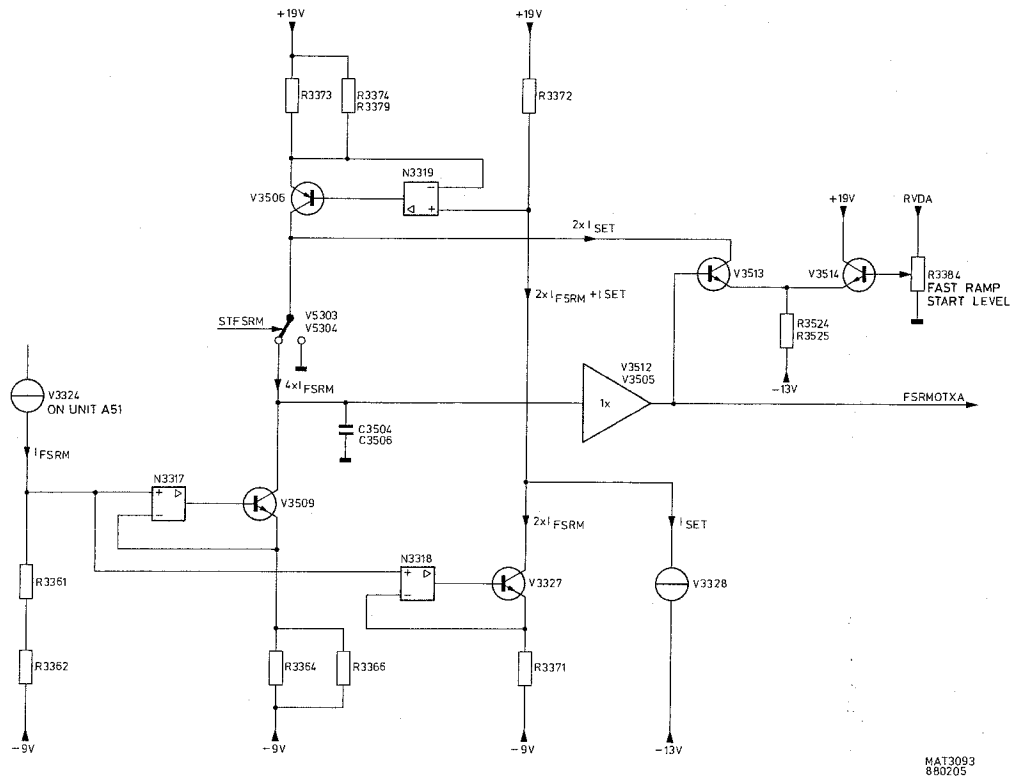


Figure 8.51.2 Block diagram fast ramp generator.

After a trigger, the STFSRM signal changes over the switch, consisting of transistors V3503 and V3504.

Now the current from transistor V3506 is led to ground and the current, which is sunk by transistor V3509 discharges the time-base capacitors linearly.

The signal FSRMOTXA is a decreasing fast ramp. When the signal crosses the end level, the hold off time starts. Now the switch of transistors V3503 and V3504 is reset via the THREE STAGE TRIGGER unit A32 and the time-base capacitors are charged again to the start level.

8.51.4 Circuit description

The FAST RAMP DAC is a serial DAC (N3313), which gets its data from the microprocessor via the Management unit A25. The output current at pin 22 is amplified by the circuitry around opamps N3314, N3316 and transistors V3323 and V3324.

The output current FSRMCU controls the steepness of the fast ramp of the FAST RAMP GENERATOR, which is described in the previous section. The slope of the fast ramp can be fine adjusted with C3506.

In the time-base settings 200 ns/div...20 us/div, capacitors C3508, C3509 and C3510 are switched parallel to the capacitors C3504 and C3506 by transistor V3511. This transistor is used in a reverse way to get a lower on-resistance.

The FAST RAMP/STAIR COMPARATOR compares the output voltage of the fast ramp generator (FSRMOTXA) with the output voltage of the STAIR ATTENUATOR (STOT--XA). It is a fast symmetrical schmitt trigger circuit, consisting of transistors V3541, V3542, V3538, V3539, V3536, V3537 and associated circuitry. The transistors V3543 and V3544 form an output buffer.

If the fast ramp voltage goes below the stair voltage then transistor V3536 blocks and V3537 conducts. Now transistor V3543 conducts, which makes STSAGT high. STSAGT is applied to the Gate unit A54 and causes that a sample of the input signal is taken. The STSAGTLT signal informs the A.C.L. on unit A5 that a sample is taken.

If the first sample of a scan is to be taken and the FAST RAMP GENERATOR is waiting for a start signal, then STOT--XA is just a bit lower as FSRMOTXA. To avoid the change over of the FAST RAMP/STAIR COMPARATOR, due to interference, the circuit around transistors V3350, V3351 and transformer T3501 decreases the voltage at the base of transistor V3537 in this situation.

The END OF FAST RAMP COMPARATOR detects the crossing of the end level of the fast ramp voltage. If the FSRMOTXA voltage goes below -3 Volt, which is determined by zenerdiode V3520, then transistor V3517 conducts and sets the HOLD OFF FLIPFLOP via transistor V3519, which starts the hold off time.

The HOLD OFF FLIPFLOP is a fast flipflop consisting of transistors V3521, V3522, V3523, V3526, V3527, V3529 and associated circuitry. The transistors V3528, V3568 and V3569 are output buffers. During the hold off time the status of the transistors is as given in the table below.

Conducts	Blocks
V3523	V3522
V3526	V3527
V3529	V3528
V3569	V3568
V3521	

The output signal HDOF is applied to the Three Stage Trigger unit A32, where trigger pulses are blocked during the hold off time.

At the end of the hold off time the EOHDOF signal resets the HOLD OFF FLIPFLOP via transistor V3524. Now the RSHDOF signal resets the hold off timer circuit.

The SYNC SWITCH switches capacitor C3517 between the HDOF signal and ground in SYNCHRONIZE mode. So the edges of the HDOF signal are made less steep. The capacitor is switched by transistor V3533 on the SYMO--LT signal. The transistor is used in a reverse way to obtain a low on-resistance.

The HOLD OFF DAC, the HOLD OFF INTEGRATOR and the HOLD OFF COMPARATOR form the hold off timer.

The HOLD OFF DAC is a serial DAC (N3309), which gets its data from the microprocessor via the Management unit A25. The output current at pin 22, which determines the hold off time, is applied to the HOLD OFF INTEGRATOR, which consists of opamps N3311, N3312 and transistors V3317 and V3314. The output current of transistor V3317 charges capacitor C3387. This capacitor can be discharged by transistor V3314, to reset the integrator.

In some lower resolution modes the DPU needs more time to calculate interpolated samples. Therefore capacitor C3390 can be switched parallel by transistor V3316 to obtain longer hold off times. This transistor is used in reversed way to get a lower on-resistance.

The HOLD OFF COMPARATOR determines if the voltage from V3317/C3387 exceeds a level determined by the resistors R3412 and R3413. If this happens EOHDF goes high, which resets the HOLD OFF FLIPFLOP. This resets the HOLD OFF INTEGRATOR via the RSHDOF signal by discharging C3387 via transistor V3316. The integrator is also reset by RSSTCNHT if the STAIR COUNTER is reset at the end of a scan.

The TIME-BASE LATCH is a shift register (D3304), which latches a number of time-base status signals, which come from the microprocessor via the Management unit A25.

The TRIGGER DELAY DAC is a serial DAC, which gets its data from the microprocessor via the MANAGEMENT unit A25. The output current at pin 22 of N3306 is converted into a voltage by opamp N3307 and amplified by opamp N3302 and associated circuitry. Next this voltage is added to the STAIR ATTENUATOR output voltage together with -8 Volt, which comes via R3310 and R3311, and inverted by opamp N3308 (ADD+INVERT). The RC combination R3324 and C3329 is a low pass anti-noise filter. Opamps N3301 and N3302 and associated components form a highly stable reference voltage source for the STAIR DAC and the start level of the FAST RAMP GENERATOR.

The stair voltage is generated via the STAIR COUNTER, the STAIR DAC and the STAIR ATTENUATOR.

The STAIR COUNTER (D3302) gets its counting pulses (CNSTCNLT) and its reset signal (RSSTCNLT) from the A.C.L. on unit A5.

By removing jumper X3301 the count pulses can be blocked, which is used for adjustment purposes.

The output lines go to a parallel DAC, the STAIR DAC (N3304). The output currents of the DAC are converted into a voltage by opamp N3303. When the STAIR COUNTER receives count pulses, the voltage at pin 7 of N3303 is a stair case voltage, ranging from 0 to 4 volt in steps of 8 mV.

This stair case voltage can be attenuated by a resistor network, the STAIR ATTENUATOR. The output voltage is applied to the ADD INVERT circuit.

The relays, which determine the attenuation factor, are controlled by the TIME-BASE LATCH.

Note: These units forms together with the Three Stage Trigger unit A32 a closed loop (see figure (8.51.1)). When a unit hangs up, the loop can be opened by disconnecting the coax cable at X5202 on unit A32 (HDOF).

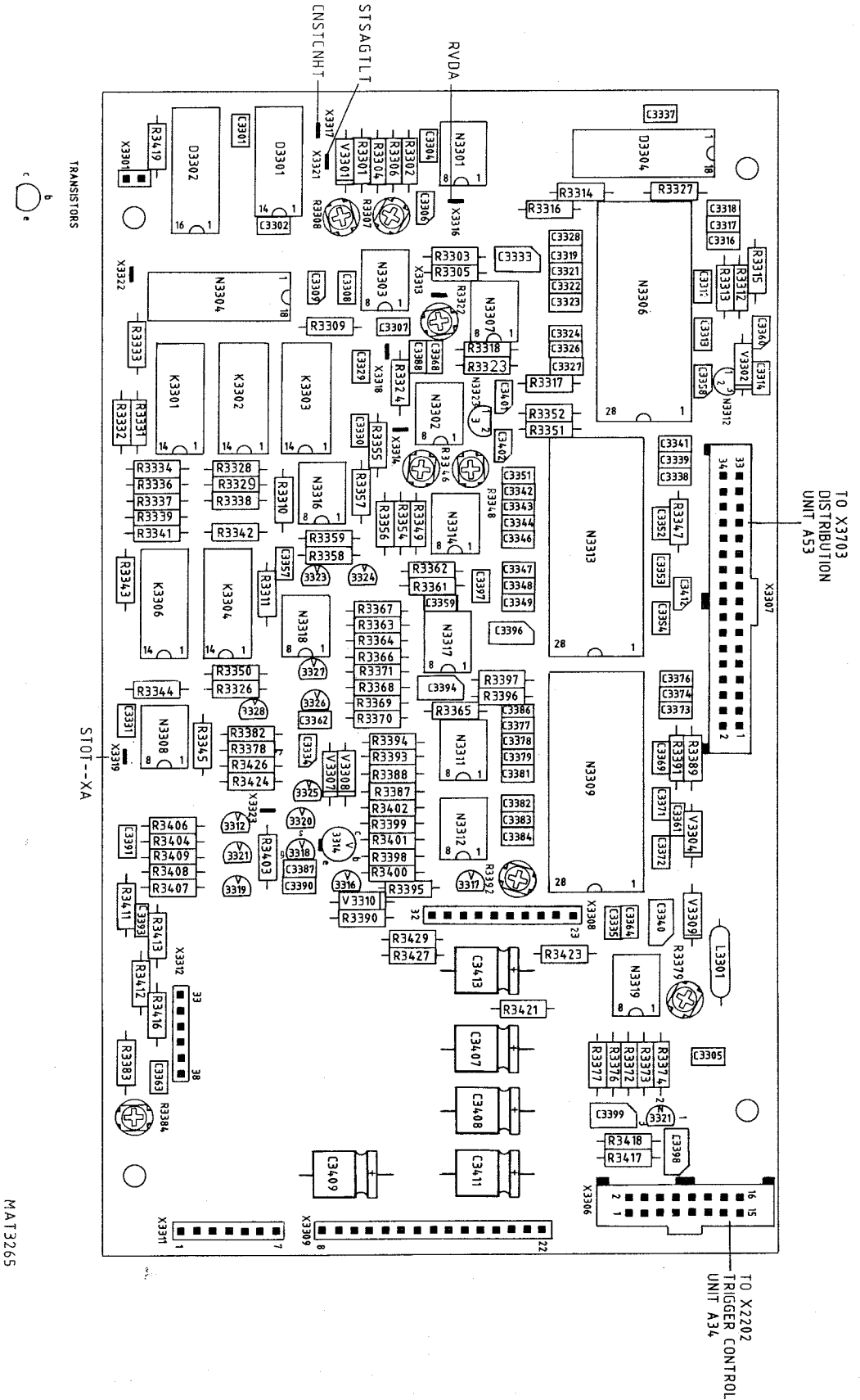
By applying a square wave of 1 kHz with an amplitude of 400 mVp-p symmetrically around zero to X5202 the correct operation of these units can be checked, if an input signal is present to generate triggers.

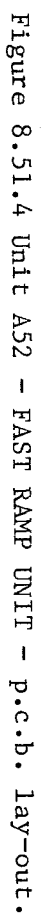
8.51.5 Signal name list

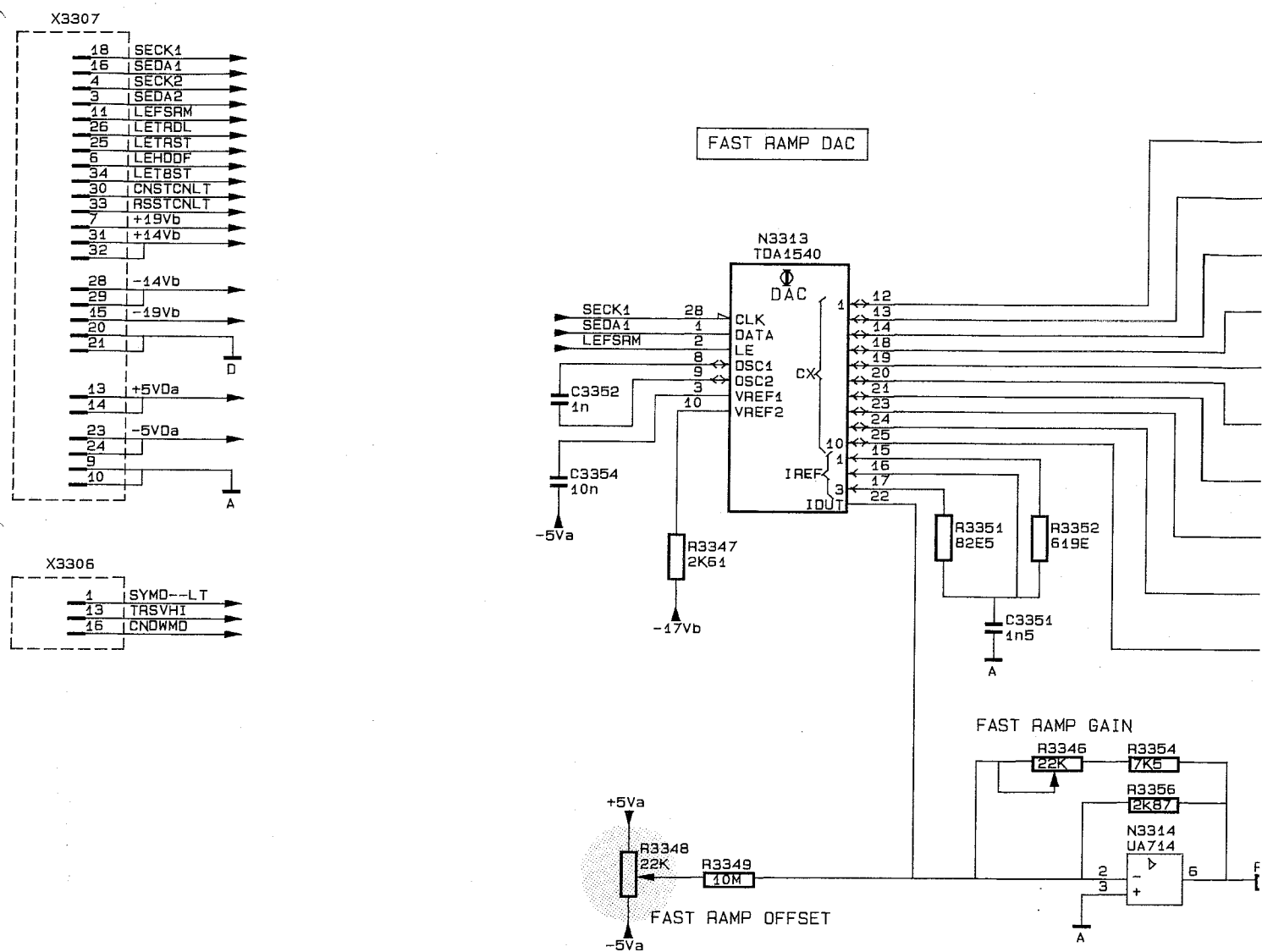
UNIT 51 (including UNIT A52)

Signal name	Description	Signal source	Signal destination(s)
CNDWMO	Count down mode	A34	-
CNSTCNLT	Count stair counter	A5	-
EOHDOF	End of hold off	A51	A52
FSRMCU	Fast ramp current	A51	A51
FSRMOTXA	Fast ramp output	A52	A52
HDOF	Hold off	A52	A32
LEFSRM	Latch enable fast ramp	A25	-
LEHDOF	Latch enable hold off	A25	-
LETBST	Latch enable time-base status	A25	-
LETRDL	Latch enable trigger delay	A25	-
LETRST	Latch enable trigger status	A25	-
RSHDOF	Reset hold off	A52	A51
RSSTCNHT	Reset stair counter	A51	A51
RSSTCNLT	Reset stair counter	A5	-
RVCUSO	Reference voltage current sources	A51	A51, A52
RVDA	Reference voltage DAC	A51	A51
SECK1	Serial clock 1	A25	-
SECK2	Serial clock 2	A25	-
SEDA1	Serial data 1	A25	-
SEDA2	Serial data 2	A25	-
STOT--XA	Stair output	A51	A52
STFSRMHX	Start fast ramp	A32	-
STFSRMLX	Start fast ramp	A32	-
STSAGT	Start sampling gate	A52	A55-A54
STSAGTLT	Start sampling gate	A52	A51-A53-A25-A12-A5
SWFSRM	Switch fast ramp	A51	A52
SWHDOF	Switch hold off	A51	A51
SYMO--LT	Synchronized mode	A34	-
TRSVHI	Trigger sensitivity high	A34	-

Figure 8.51.3 Unit A51 - TIME-BASE UNIT - p.c.b. lay-out.

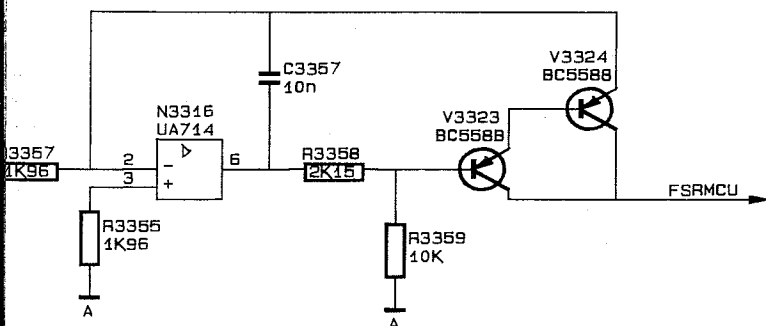
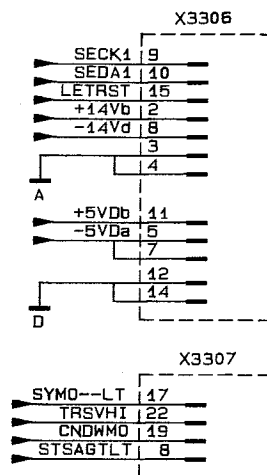
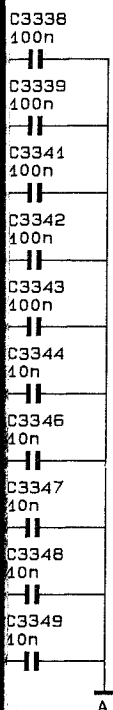




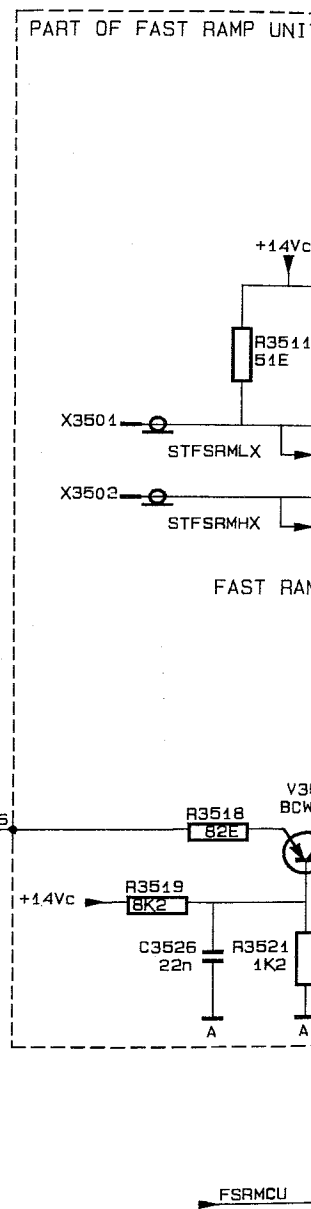


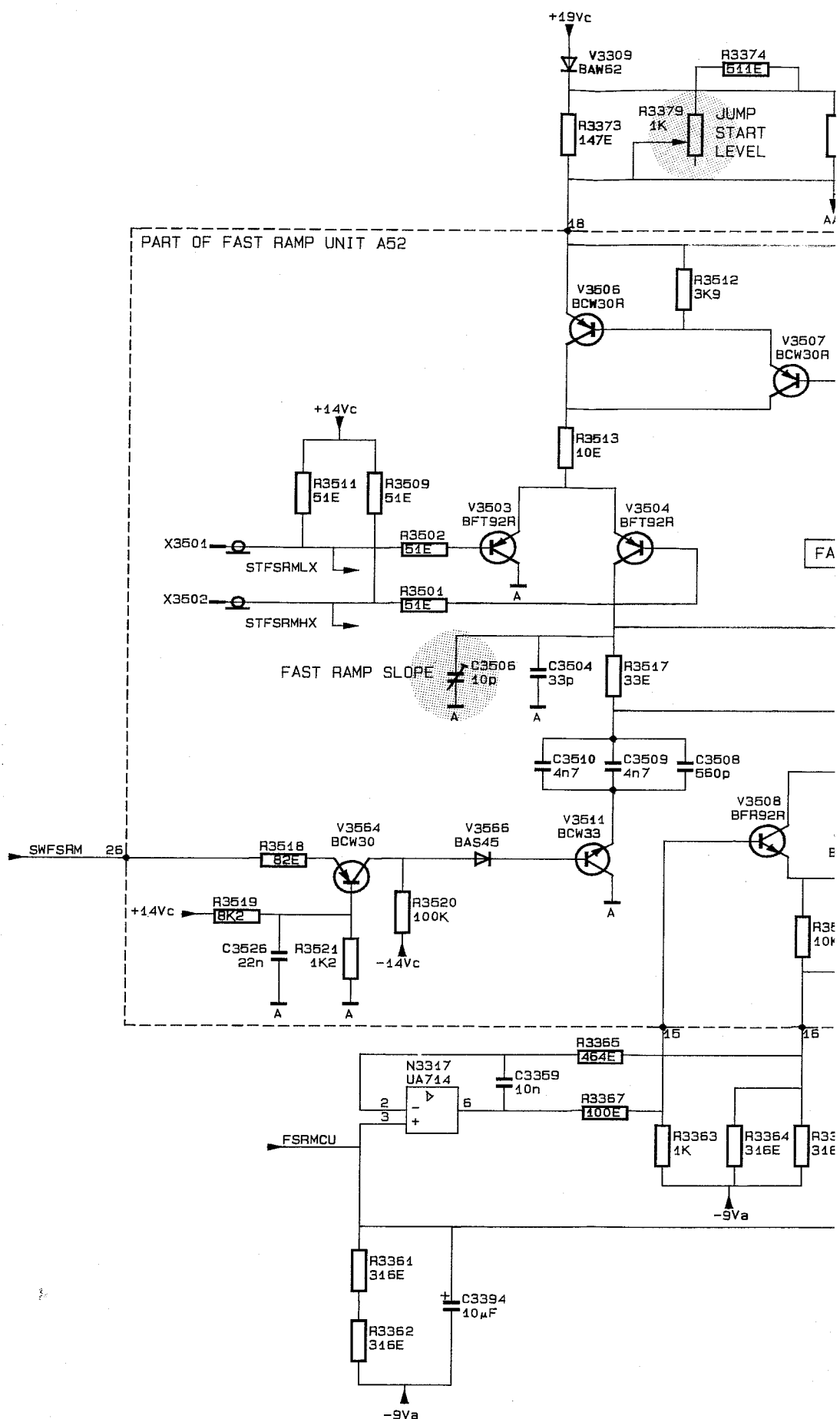
REFNR	TYPE	+5Va	-5Vb	+14Vc	-14Vc	-17Vb	I _A
N3313	TDA1540	4	7			11	6
N3314	UA714			7	4		
N3316	UA714			7	4		

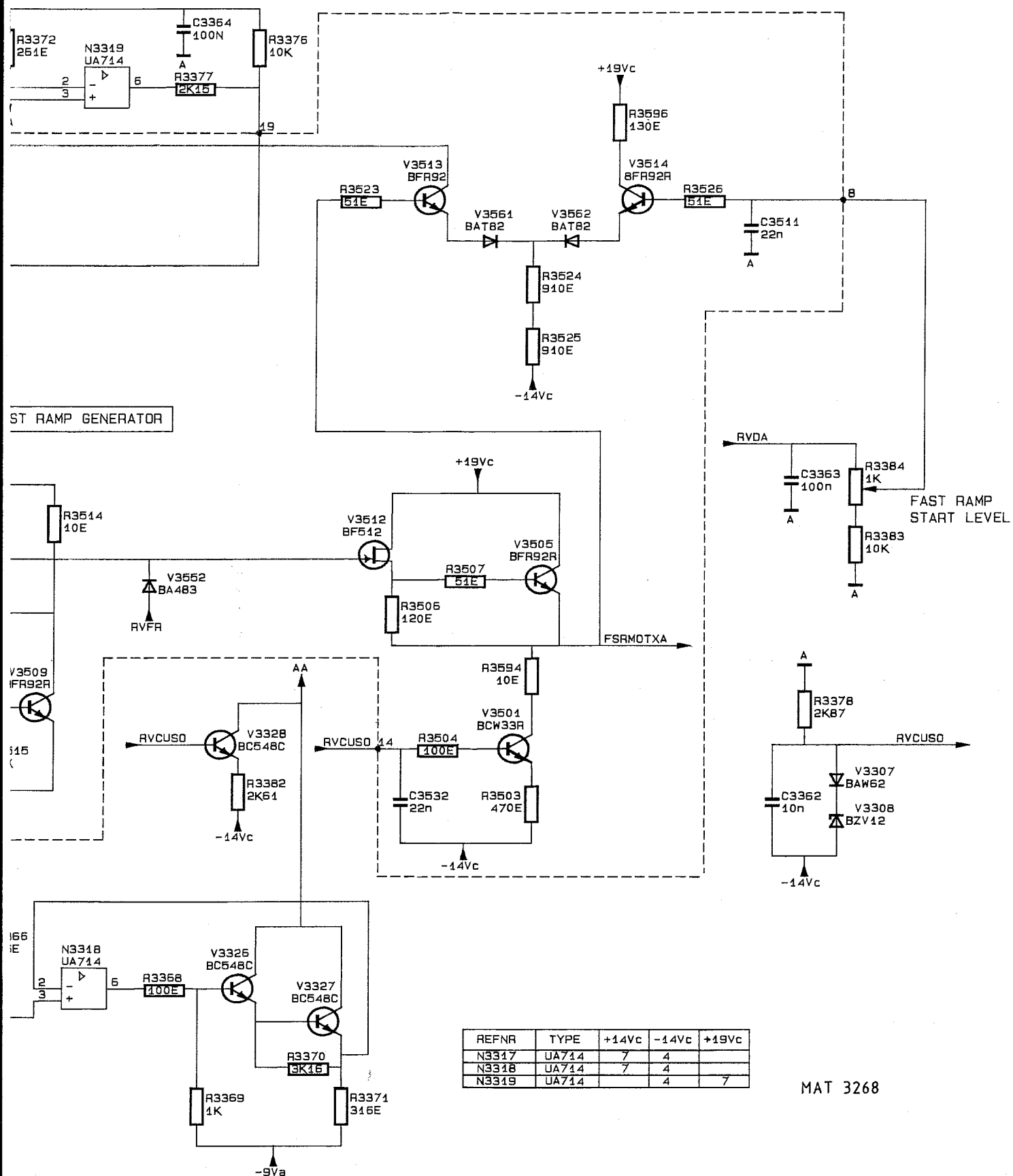
Figure 8.51.5 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.



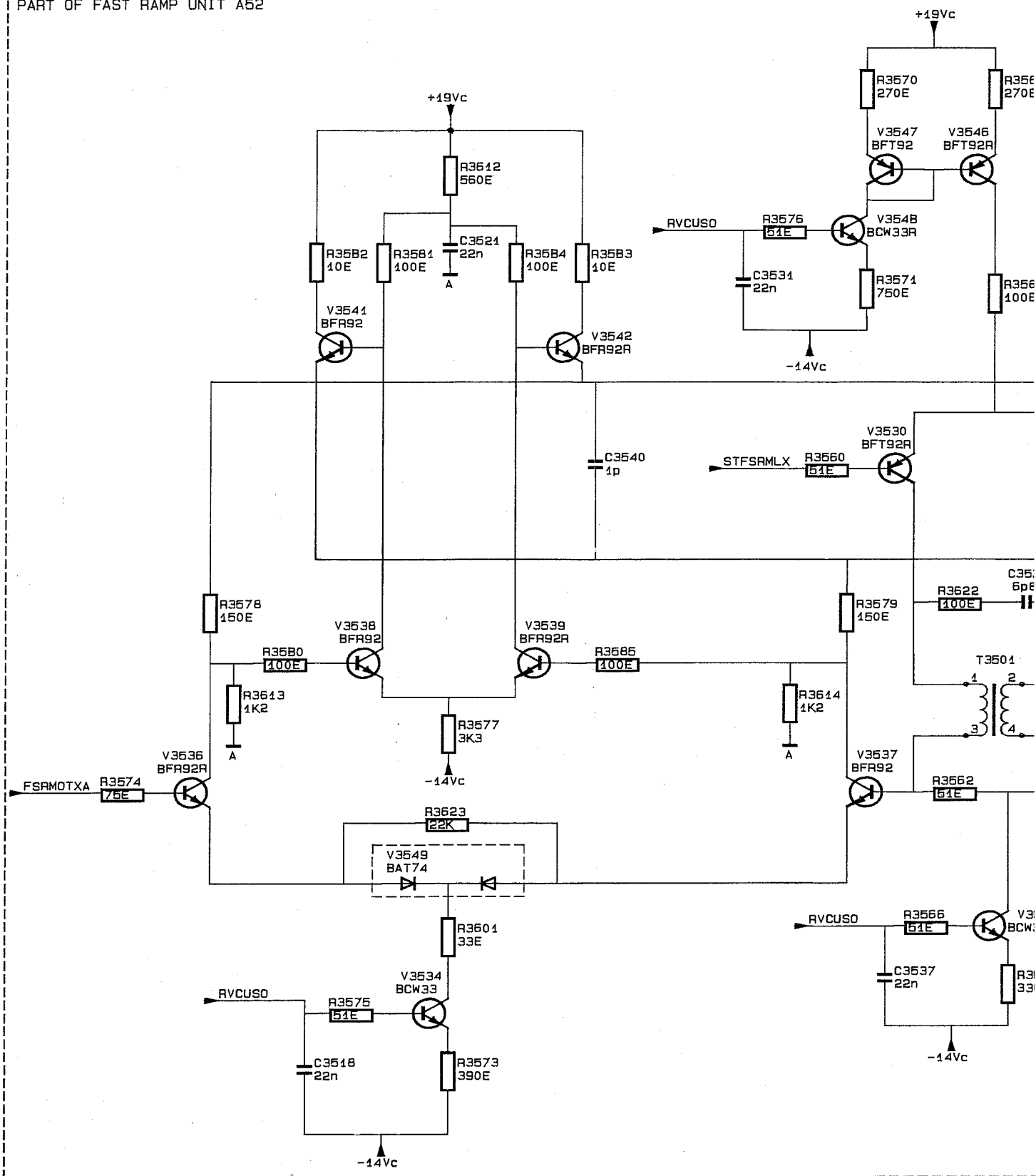
MAT 3267



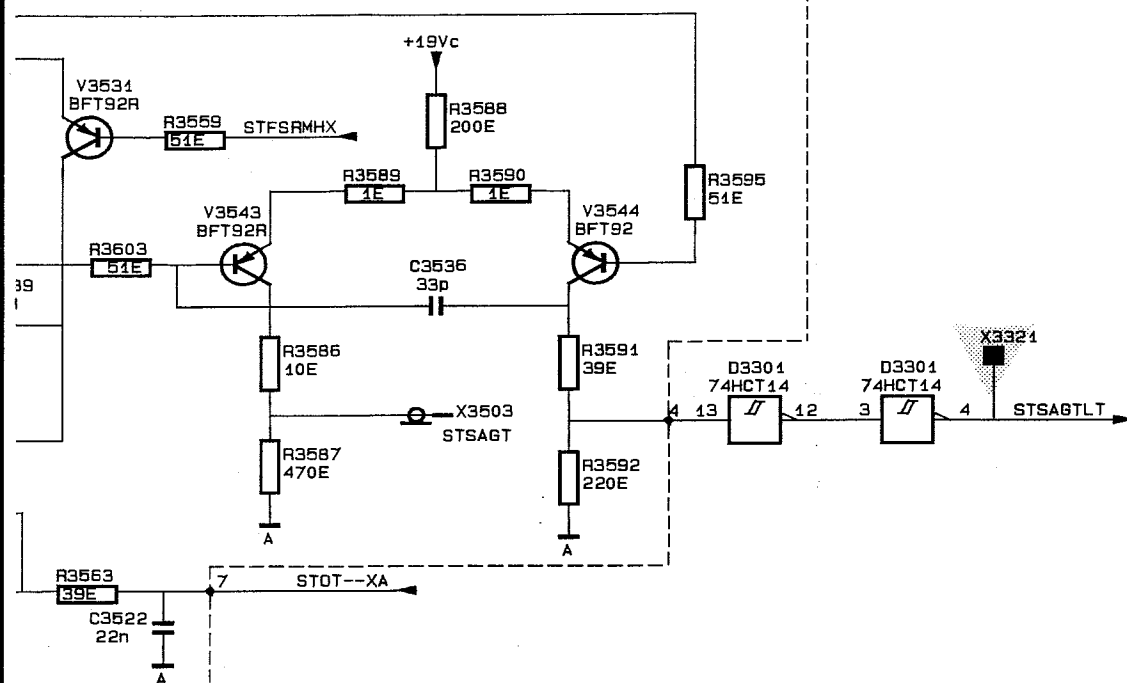




PART OF FAST RAMP UNIT A52

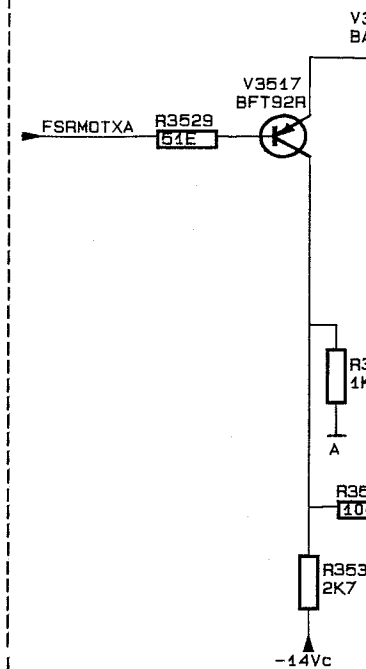


FAST RAMP/STAIR COMPARATOR



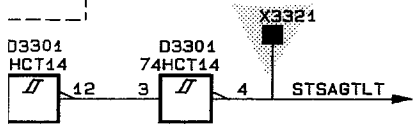
PART OF FAST RAMP UNIT A52

END OF FAST RAMP COMPARAT

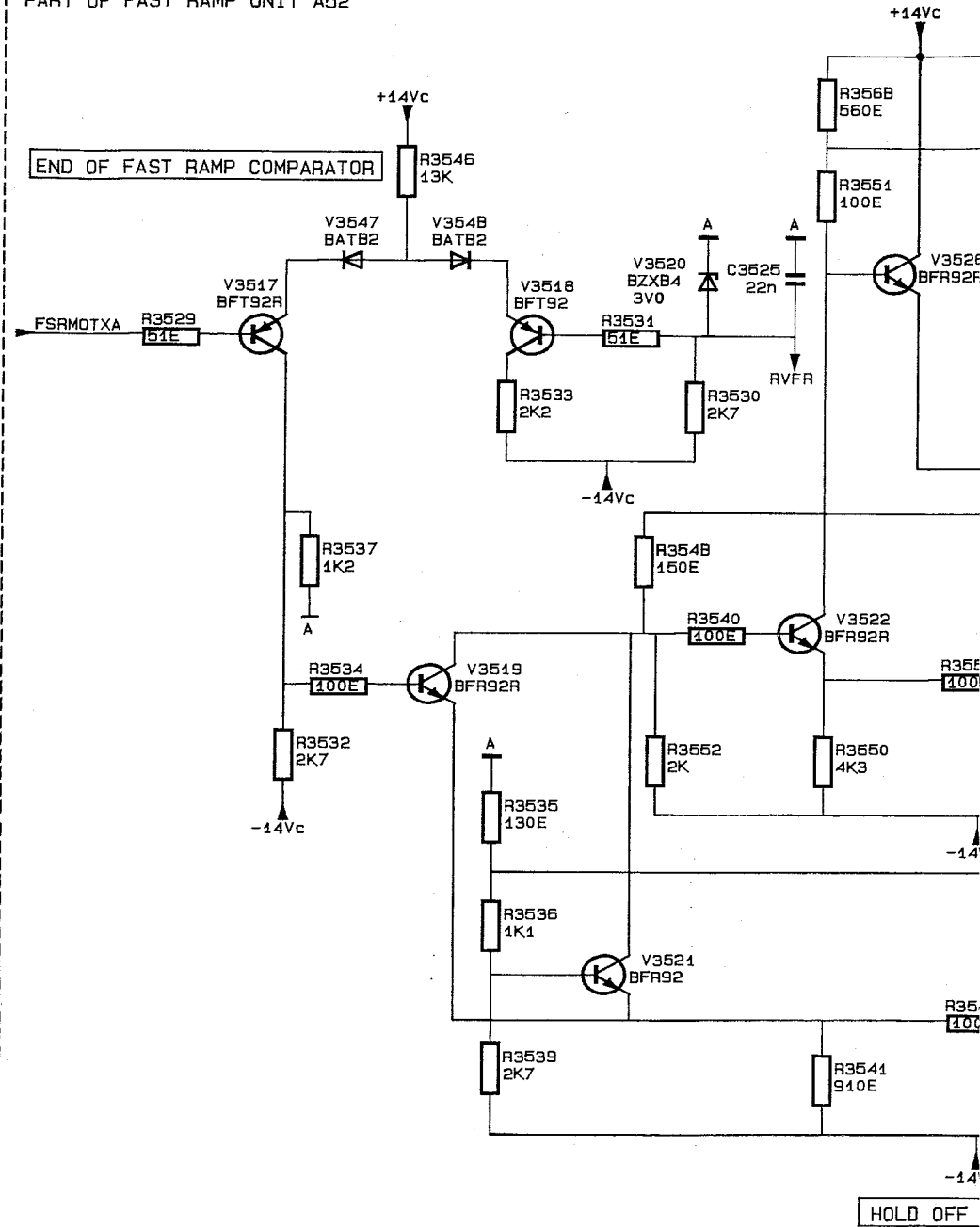


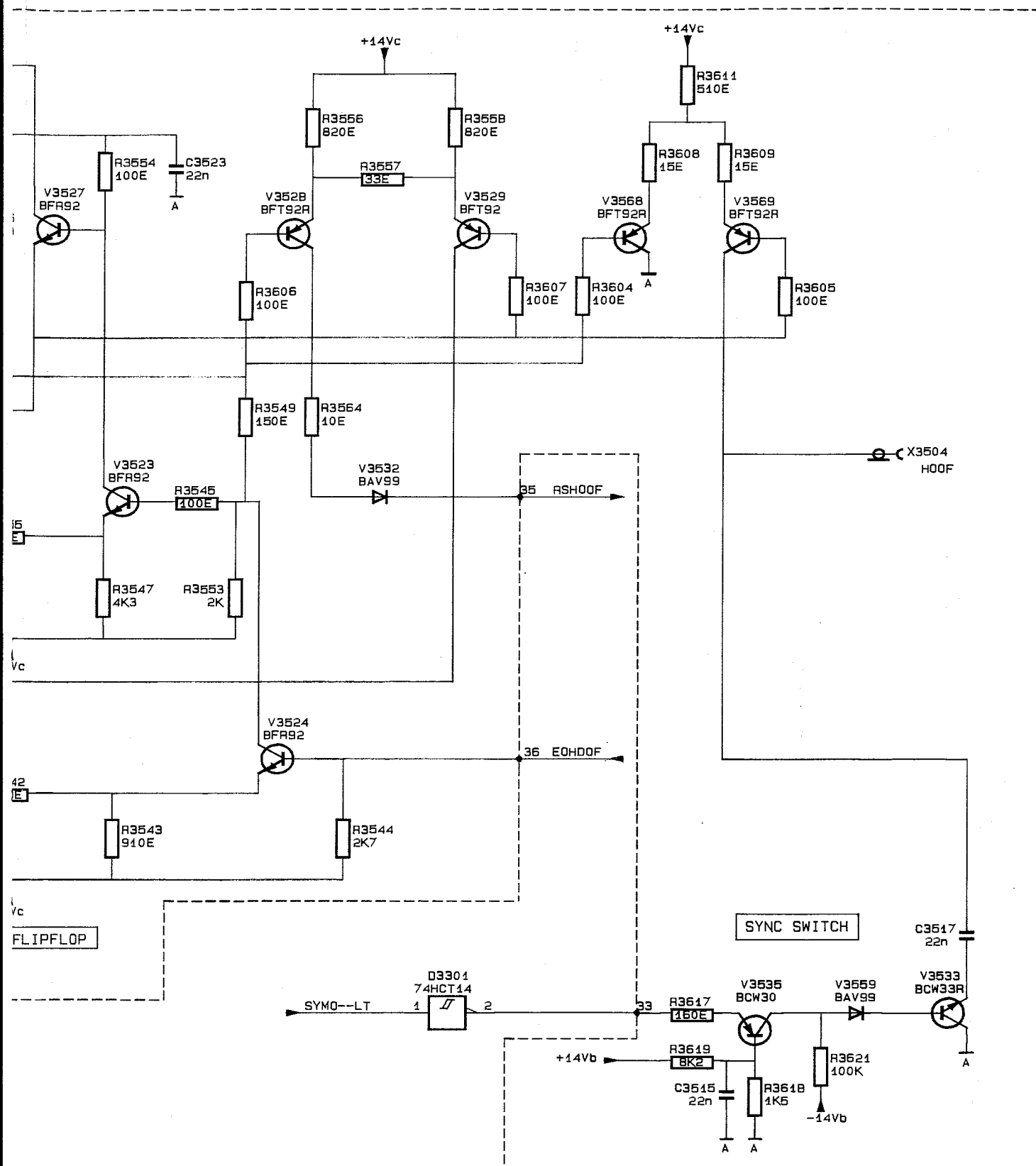
MAT 3269

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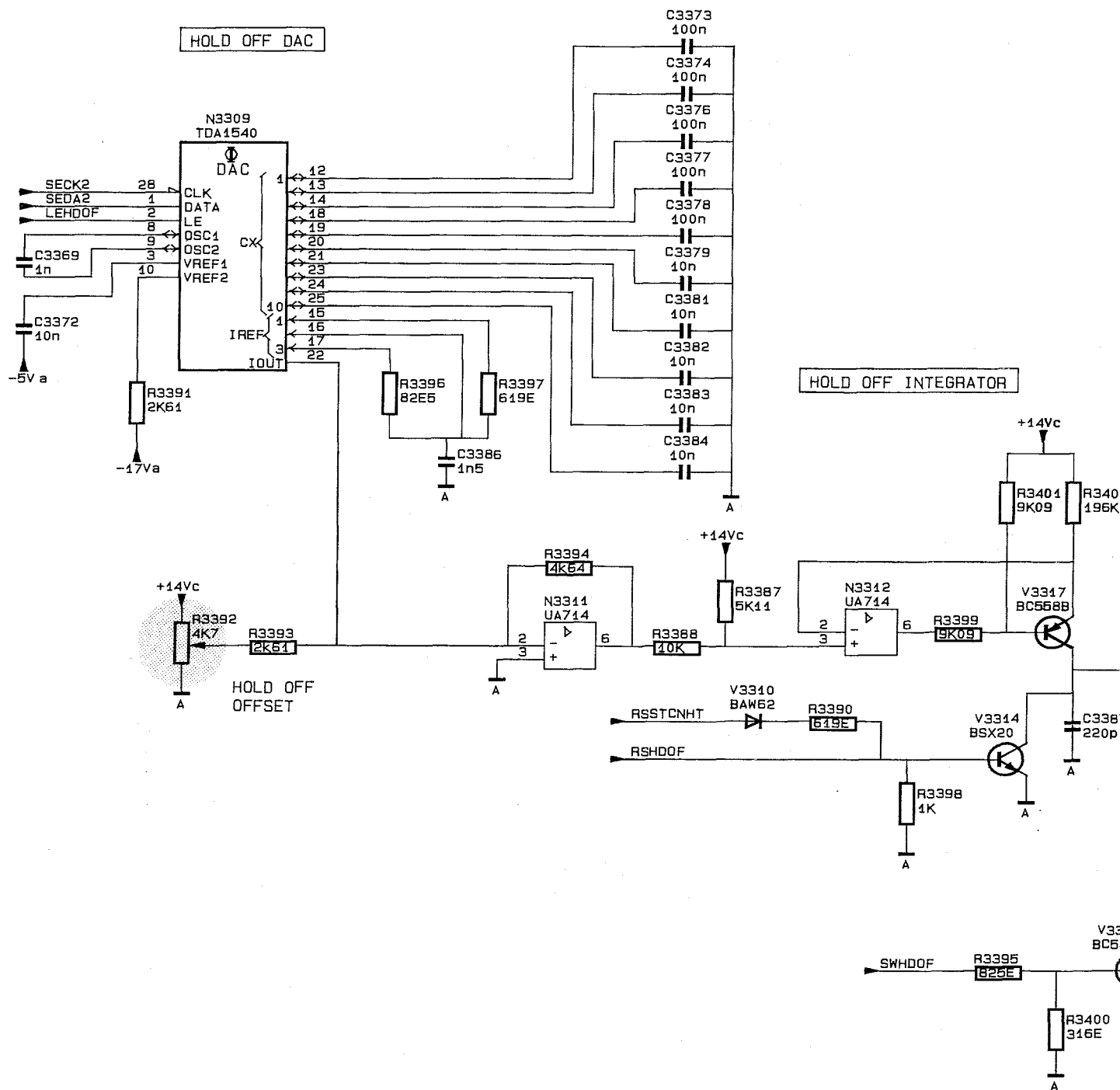
PART OF FAST RAMP UNIT A52





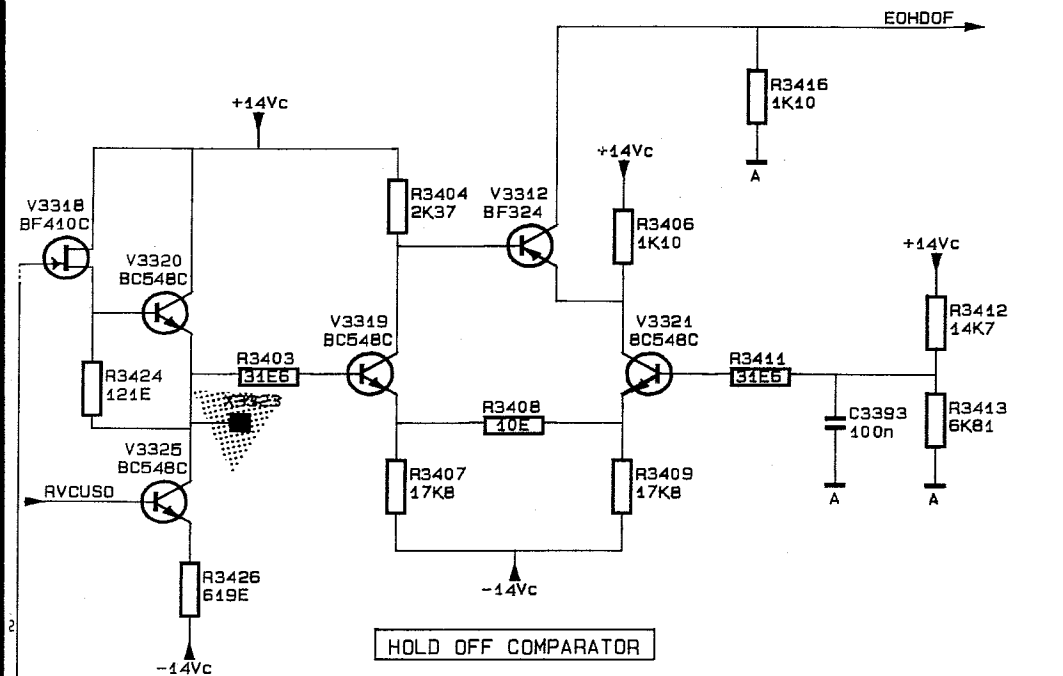
MAT 3270

Figure 8.51.6 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.

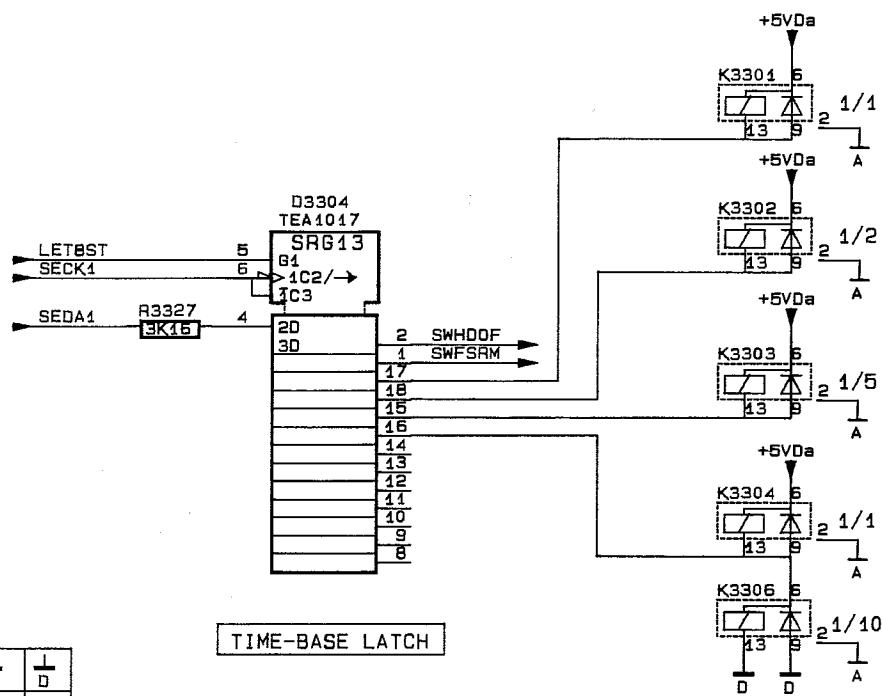


REFNR	TYPE	+5Vda	-5Va	+5Va	-14Vc
N3309	TDA1540		7	4	
N3311	UA714				4
N3312	UA714				4
D3304	TEA1017	7			

Figure 8.51.7 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.

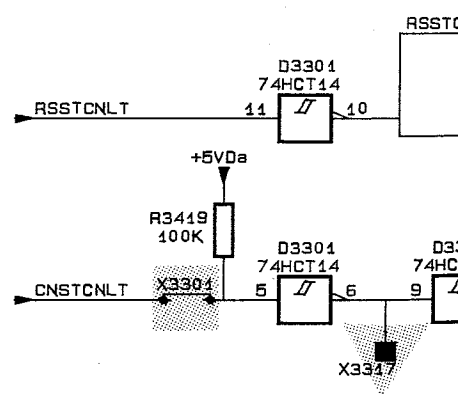
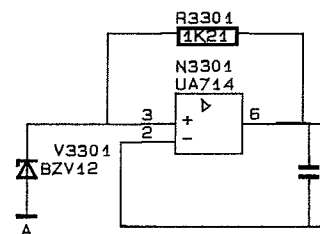
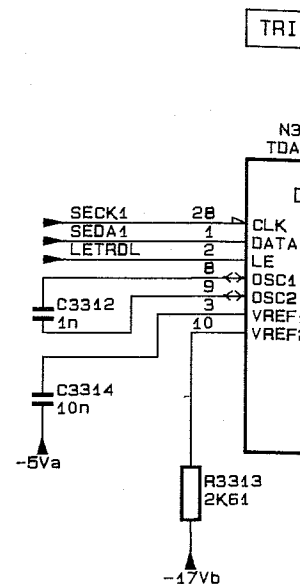


HOLD OFF COMPARATOR

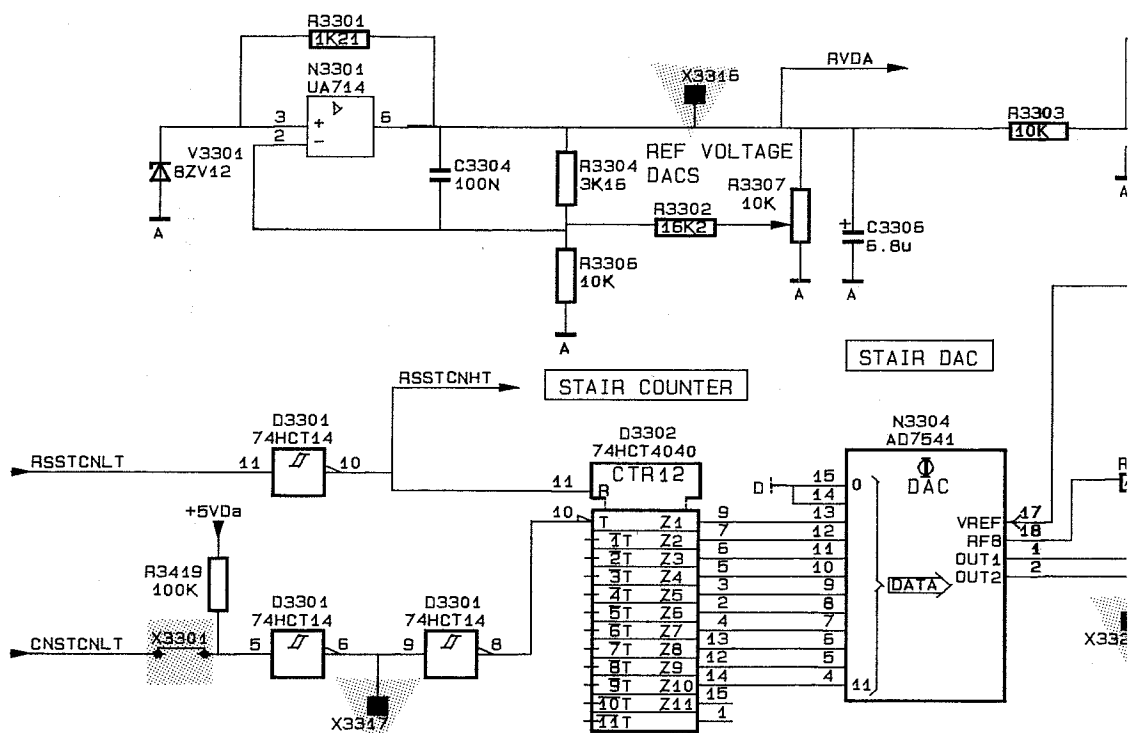
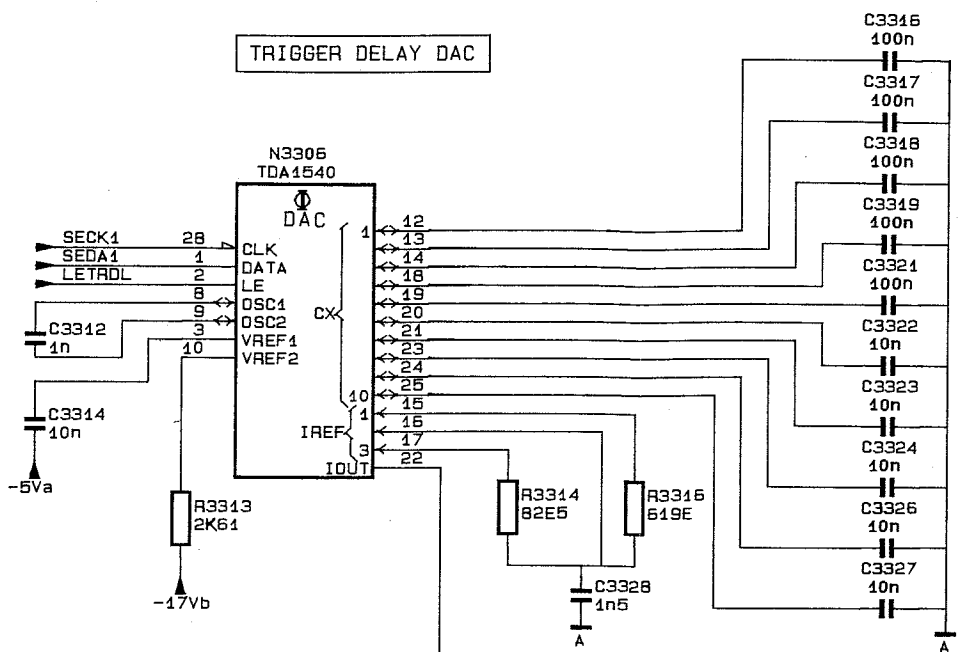


TIME-BASE LATCH

MAT 3271

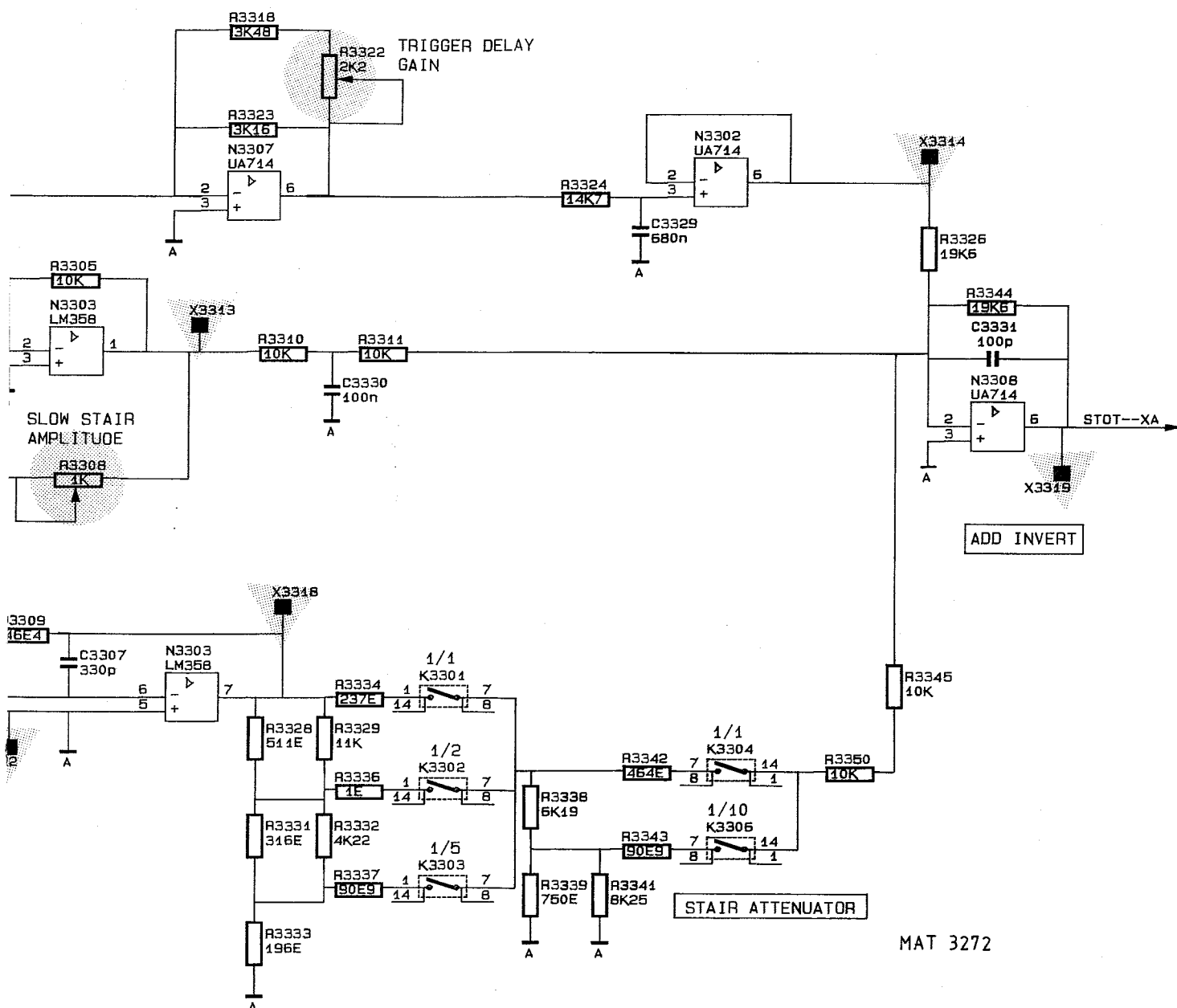


+14Vc	-17Va	1	1
	11	6	D
7			
7			
			3

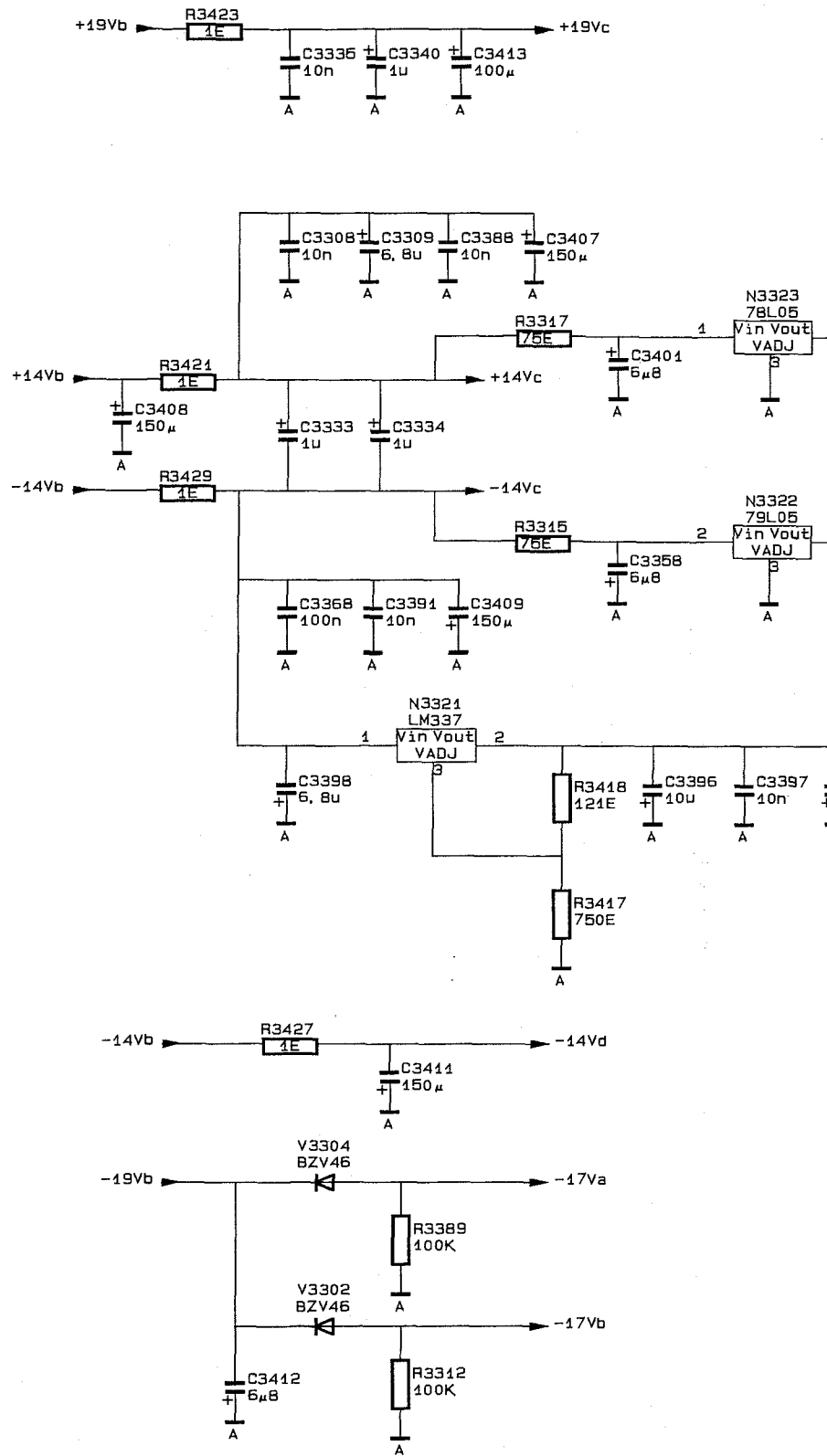


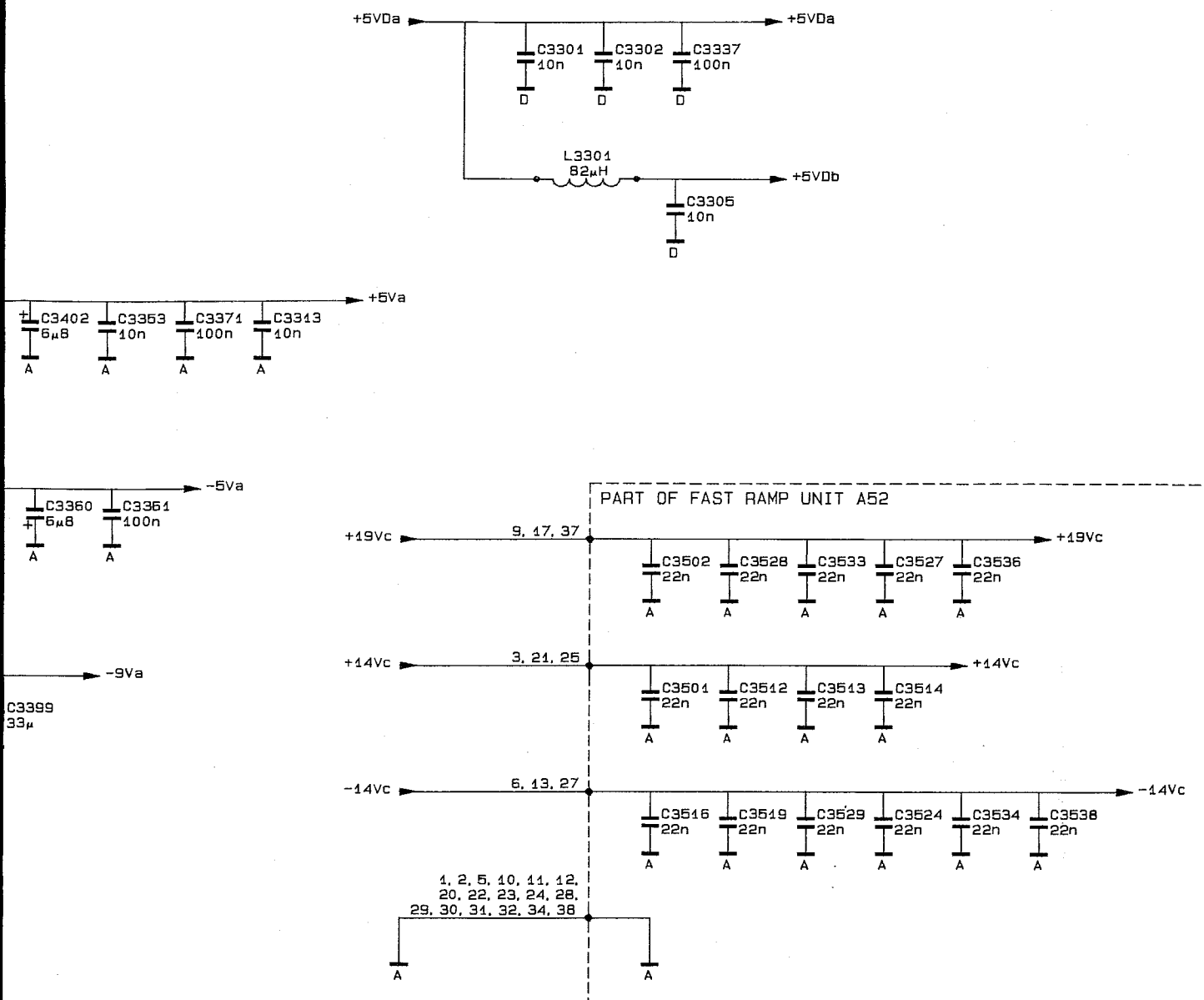
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REFNR	TYPE	+5V0a	+5Va	-5Va	+14Vc	-14Vc	-17Vb	$\frac{1}{A}$	$\frac{1}{D}$
D3301	74HCT14	14						7	
D3302	74HCT4040	16						8	
N3301	UA714				7			4	
N3302	UA714				7	4			
N3303	LM358N				8	4			
N3304	AD7541A				16				3
N3306	TDA1540		4	7			11	6	
N3307	UA714				7	4			
N3308	UA714				7	4			



MAT 3272





MAT 3273

Figure 8.51.8 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.