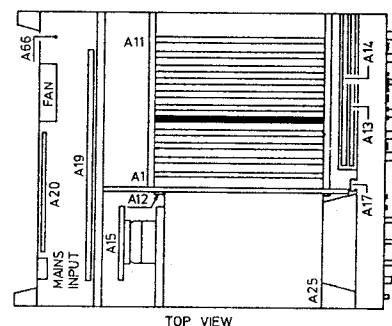


UNIT A5 - GRAM UNITCONTENTS

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8.5.2	Memory circuit.....	8.5-1
8.5.3	ACL circuit.....	8.5-2
8.5.4	Signal name list.....	8.5-4

8.5.1 General information

This unit basically consists of the microprocessor memory circuit (RAM) and the acquisition control logic (ACL).

8.5.2 Memory circuit

The microprocessor memory circuit consists of a RAM and some control logic.

The RAM consists of RAM0 (D1834 and D1836), which is backed up by the battery, and RAM1 (D1837 and D1838). All devices are 32 KByte types. If 8 KByte types are used for D1834 and D1836, then soldering joint J1801 should be changed over.

The ADDRESS REGISTER latches the data of the microprocessor address lines. It is clocked by CKAB--HT, which is active when addresses on the address bus are stable.

The BIDIRECTIONAL DATA buffer buffers the data lines to the microprocessor. It is enabled by CKAB--LT. The direction of data transfer is determined by RARD--LT.

The SELECT LOGIC generates the RAM select signals.

When the power goes down, MYSLDWLT goes low. Now D1833 separates SL00LOLT and SL00HILT from the select logic and so they go to VBBa level. The RAMs (only RAM0) are deselected, their contents remain.

The remaining select logic generates delayed CKAB signals and DATRAKLT, when this unit is selected.

The delay of the CKAB signals (R1802 and C1892) ensures stable data on the address bus and the data bus when they are clocked in.

The delay of DATRAKLT (R1839 and C1893) ensures enough data setup time for the RAM.

8.5.3 ACL circuit

The ACL circuit consists of the following parts:

- ACL latch
- ACL reset logic
- Acquisition Control Logic (ACL)

The ACL latch is a shift register (D1814), which latches a number of ACL status signals, which come from the microprocessor via the MANAGEMENT unit A25.

The ACL RESET LOGIC generates reset signals for the ACL (RSACL and RSACL-LT) and the reset signal for the stair counter (RSSTCNLT) on the Time-base unit A51. The ACL is reset by the CLACL signal from the ACL LATCH, when a new setting of the instrument is made, or by the TRRY signal from the DPU Control unit A8. TRRY marks that the DPU is ready to accept a new sweep of samples.

The stair counter is reset by RSSTCNLT, when IL02--LT from the DPU CONTROL goes low (D1820). IL02--LT marks that the DPU has accepted a sweep of samples.

The ACQUISITION CONTROL LOGIC generates the required signals for the control of the capture of samples.

These signals are:

Name	Description	Destination
HDSA-1	Hold sample	Vertical signal unit A55
CNSTCNLT	Count stair counter	Time-base unit A51
STCV	Start conversion	ADC + T&H unit A11
CHPT	Channel pointer	DPU control unit A8
CHSW	Channel switch	Vertical signal unit A55
DAVA	Data valid	DPU control unit A8
TKSA	Take sample	DPU control unit A8
EODA	End of data	GRAM unit A5

The HDSA-1 signal generates THMOA and THMOB via the TRACK & HOLD CONTROL on the Vertical Signal Unit A55.

The time T1 consists of a short time made on this unit (determined by R1841 and C1861) and the HOLD DELAY times on unit A55.

In the timing diagram it is assumed that:

- Channels A and B are selected
- Multiple sampling is off
- The screen resolution is 512 dots

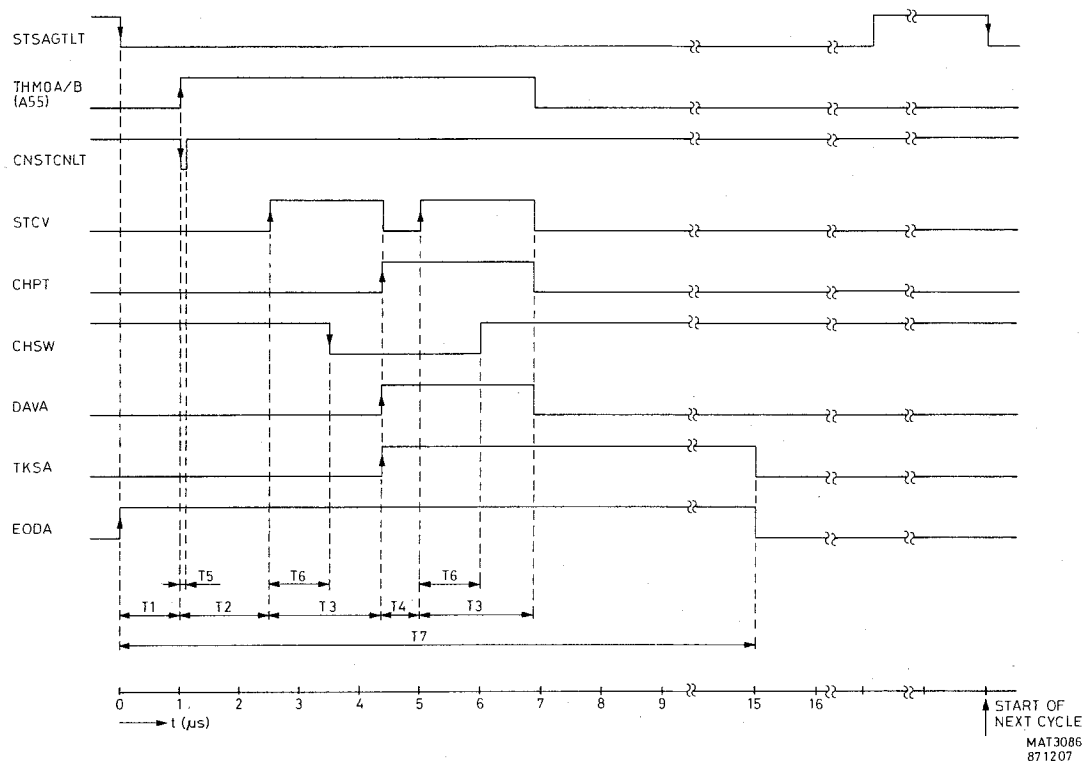


Figure 8.5.1 Timing diagram of acquisition control signals

On the falling edge of STSAGTLT, a sample is taken in the Gate unit A54, and amplified on the Vertical Signal unit A55. After a time ($T1$) the sample value is stable at the TRACK & HOLD on the Vertical Signal unit and THMOA and THMOB go high to hold the sample.

Next a count pulse ($T5$) for the STAIR COUNTER (CNSTCNLT) is generated to prepare the Time-base unit A51 for the next sample.

After a time ($T2$) the TRACK & HOLD is settled and STCV goes high to start conversion of the sample of channel B on the ADC unit A11. After the conversion time ($T3$) the ADC needs some time to reset ($T4$) before the sample of channel B can be converted.

Because the ADC unit has also a TRACK & HOLD circuit, the CHANNEL SWITCH on the Vertical Signal unit may change over as soon as this T&H is in hold mode. This is timed out by $T6$.

The DAVA signal, which marks to the DPU that valid samples come from the ADC, is only active when the first sample of a sweep is taken, otherwise it is continuous low.

The TKSA signal is only active, when a sample from the ADC should be taken by the DPU. In dual channel mode it operates like given in the diagram above.

If channel A only is selected, it goes low at the falling edge of the second STCV pulse.

If channel B only is selected, it first goes high at the falling edge of the second STCV pulse.

The EODA signal marks the time (T7) in which the above mentioned signals may be active.

The repeat time of the STSACTLT signal depends on the setting of the instrument and on the frequency of the input signal. The minimum repeat time is 35 us.

The ACL is built around a number of monostable multivibrators, which generate a pulse when they are activated. The above mentioned times T1...T7 are indicated the circuit diagrams. The remaining monostable multivibrators generate a small pulse on their activating edge.

The ADC and T & H unit A11 is clocked by the microprocessor clock. Therefore the generation of the STCV signal is synchronised by UPCK16. If Multiple Sampling is selected, e.g. 4, then every fourth sample should be taken by the DPU and next the stair counter should be incremented. This multiple sampling factor is counted up by two 3-bit counters (D1810). Via multiplexer D1811 the corrected counter line is selected to generate TKSA and CNSTCNLT.

The generation of TKSA is influenced by the signals A, B and DUAL, which depend on the selected vertical channels.

In lower resolution modes, the stair counter should be incremented 2, 4 or 8 times, depending on the selected resolution. This is counted down by counter D1813, which gets its pulses from IC D1812, which operates as a pulse generator.

8.5.4 Signal name list

UNIT A5

Signal name	Description	Signal source	Signal destination(s)
A	Channel A mode	A5	A5
AB01...16	Address bus 01...16	A6 + Option	-
AB19	Address bus 19	A6	-
B	Channel B mode	A5	A5
CHPT	Channel pointer	A5	A5, A12-A8, A12-A25
CHPT--LT	Channel pointer	A5	A5
CHSW	Channel switch	A5	A12-A25
CKAB--HT	Clock address bus	A5	A5
CKAB--LT	Clock address bus	A5	A5
CLACL	Clear acquisition control logic	A5	A5
CNSTCNLT	Count stair counter	A5	A12-A25-A53-A51
DAHISBLT	Data high strobe	A6 + Option	-
DALOSBLT	Data low strobe	A6 + Option	-
DATRAKLT	Data transfer acknowledge	A3+A5+A6+A8 + Option	A12-A6, A12-Option
DAVA	Data valid	A5	A5, A12-A4, A12-A8
DB00...15	Data bus 00...15	A6 + Option	-
DUAL	A and B mode	A5	A5

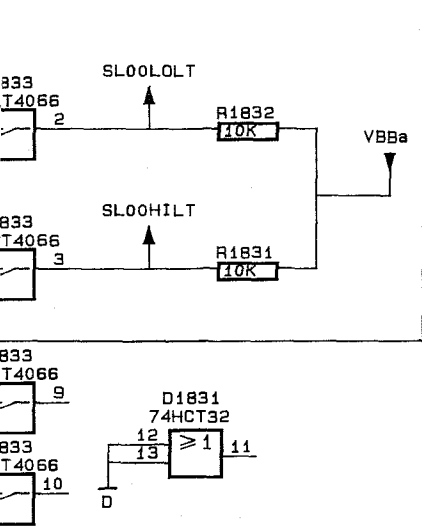
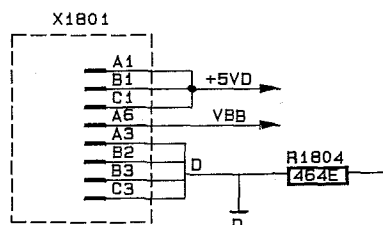
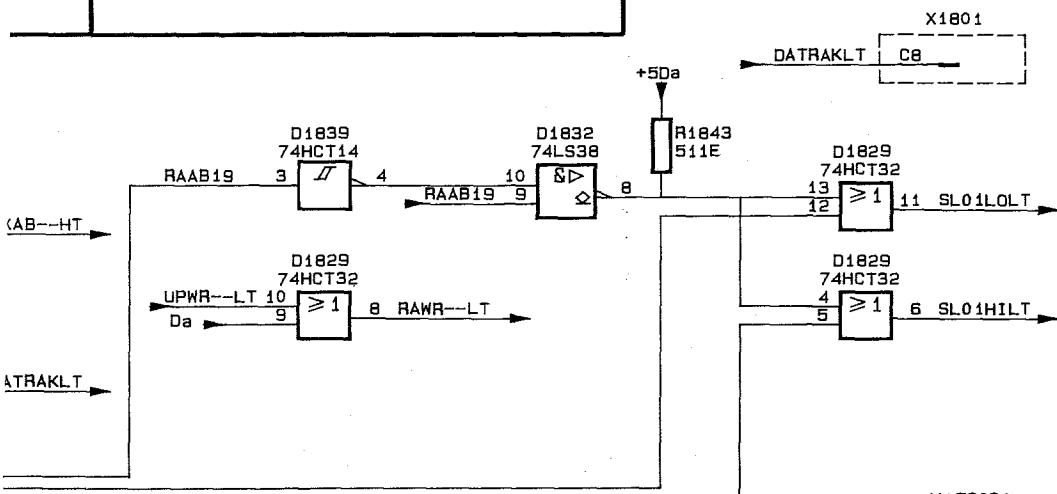
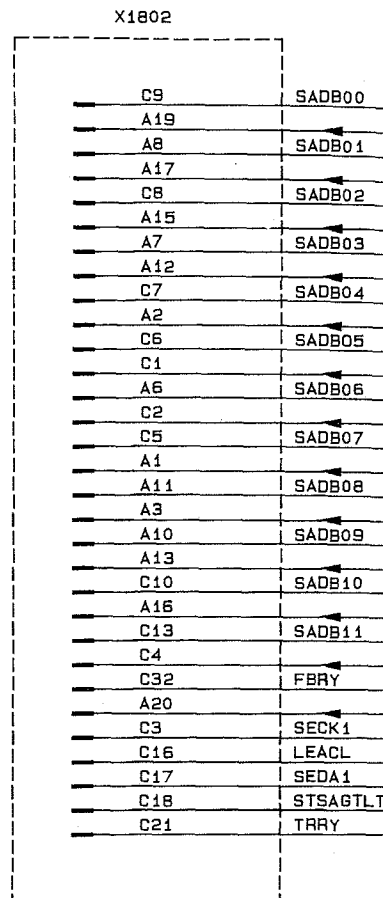
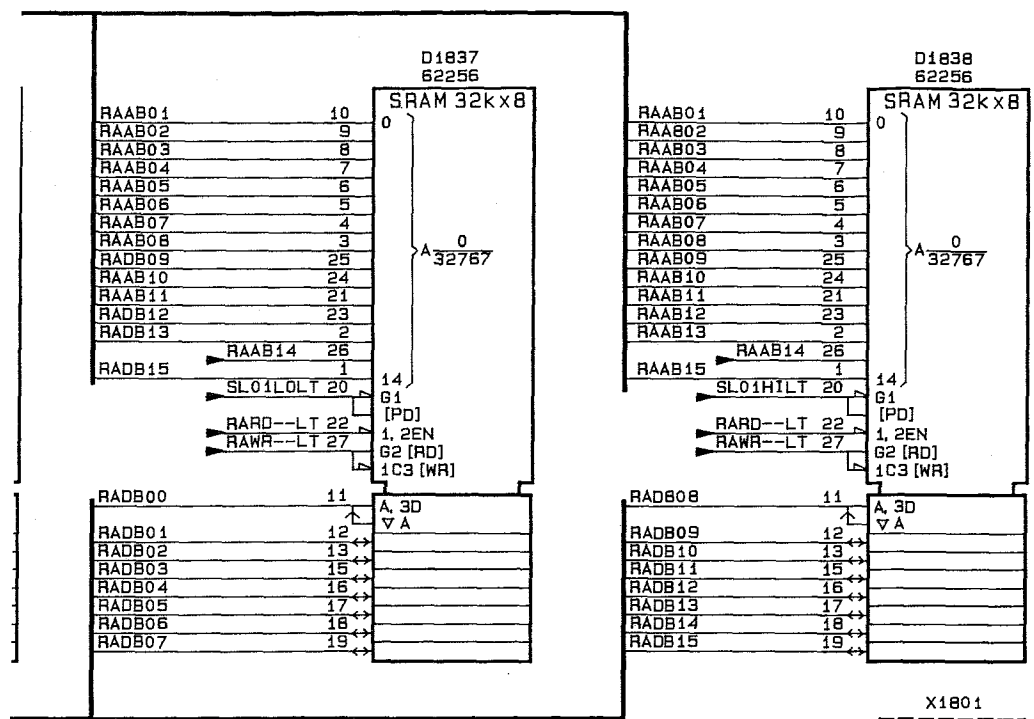
Signal name	Description	Signal source	Signal destination(s)
ENDBBFLT	Enable data bus buffer	A5	A5
EODA	End of data	A5	A5
FBRY	Feedback ready	A8	-
HDSA	Hold sample	A5	A5
HDSA-1	Hold sample 1	A5	A55
IL02--LT	Interrupt level 02	A8	-
IOSL08LT	I/O Select 08	A6	-
LEACL	Latch enable acquisition control logic	A25	-
MSC0...2	Multiple sampling control 0...2	A5	A5
MYSLDWLT	Memory select down	A6	-
MYSL01LT	Memory select 01	A6	-
RAAB01...16	RAM address bus 01...16	A5	A5
RAAB19	RAM address bus 19	A5	A5
RADB00...15	RAM data bus 00...15	A5	A5
RARD--LT	RAM read	A5	A5
RAWR--LT	RAM write	A5	A5
RSACL	Reset acquisition control logic	A5	A5
RSACL--LT	Reset acquisition control logic	A5	A5
RSC0...2	Resolution control 0...2	A5	A5
RSSTCNLT	Reset stair counter	A5	A12-A25-A53-A51
SADB00...11	Sample data bus	A9+A11	-
SECK1	Serial clock 1	A25	-
SEDA1	Serial data 1	A25	-
SL00HILT	Select ram 00 high byte	A5	A5
SL00LOLT	Select ram 00 low byte	A5	A5
SL01HILT	Select ram 01 high byte	A5	A5
SL01LOLT	Select ram 01 low byte	A5	A5
STCV	Start conversion	A5	A12-A11
STSAGTLT	Start sampling gate	A51	-
TKSA	Take sample	A5	A12-A8
TRRY	Transfer ready	A8	-
UPCK16	Microprocessor clock 16 MHz	A6	-
UPRD--LT	Microprocessor read	A6	-
UPRSOTLT	Microprocessor reset out	A6	-
UPWR--LT	Microprocessor write	A6	-
VBB	Voltage battery backup	A6	-
VBBa	Voltage battery backup a	A5	A5

Figure 8.5.2 Unit A5 - GRAM UNIT - p.c.b. lay-out.

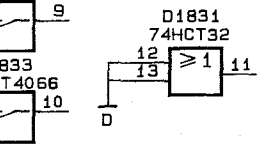
MAT 3235

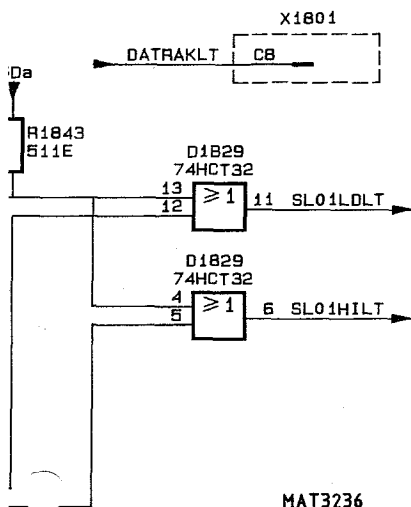
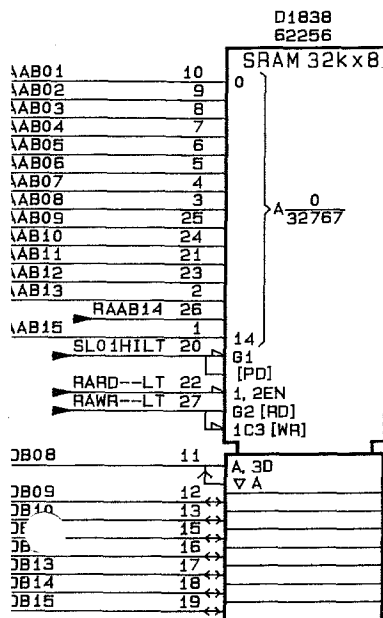


RAM 1



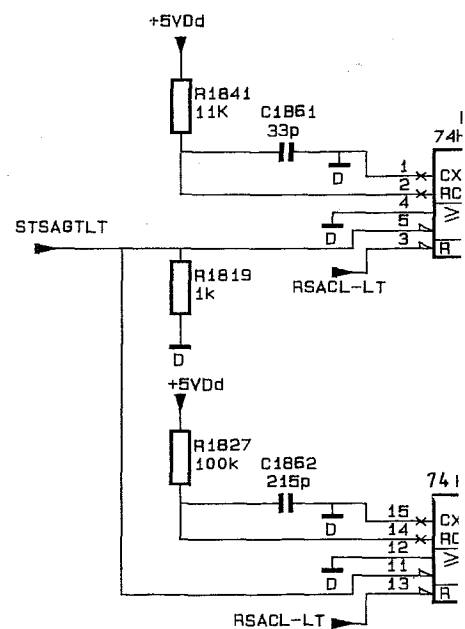
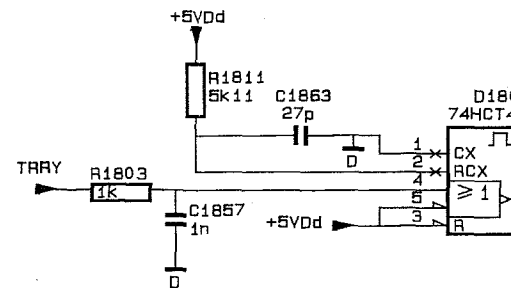
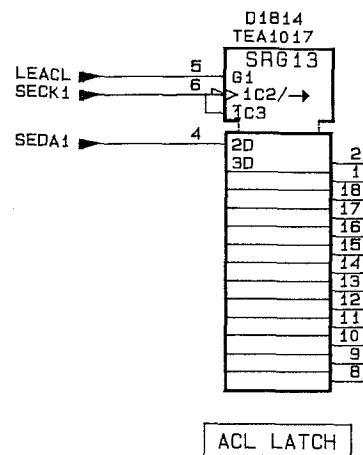
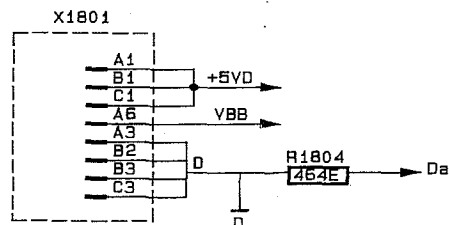
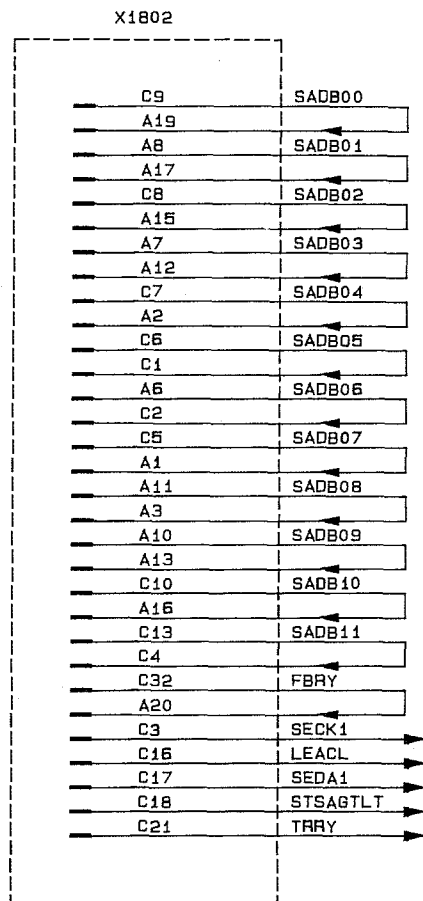
REF. NR.	TYPE NR.	+5Vda	+5Vdb	VBBa	$\frac{1}{D}$
D1823	74LS245	20	20	10	10
D1824	74LS245	20	20	10	10
D1826	74HCT574	20	20	10	10
D1827	74HCT574	20	20	10	10
D1828	74HCT573	20	20	10	10
D1829	74HCT32	14	14	7	7
D1831	74HCT32	14	14	7	7
D1832	74LS38	14	14	7	7
D1833	74HCT4066	14	14	14	14
D1834	62256	28	28	14	14
D1836	62256	28	28	14	14
D1837	62256	28	28	14	14
D1838	62256	28	28	14	14
D1839	74HCT14	14	14	7	7



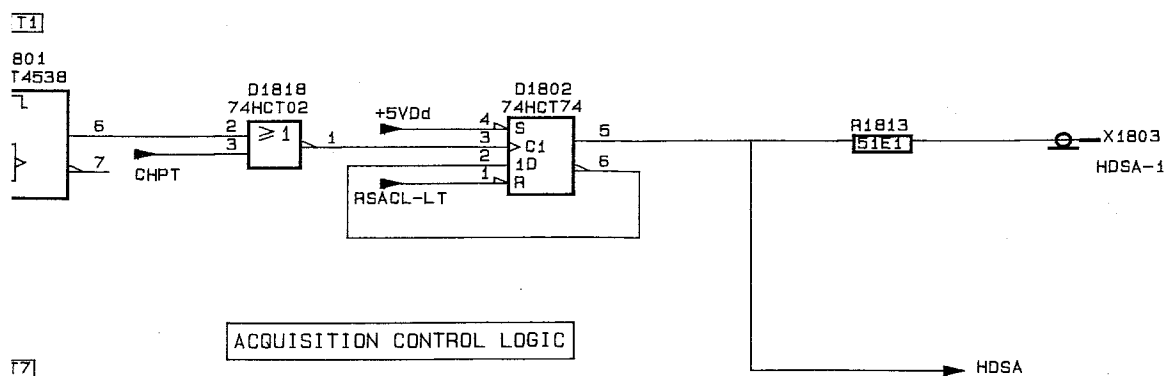
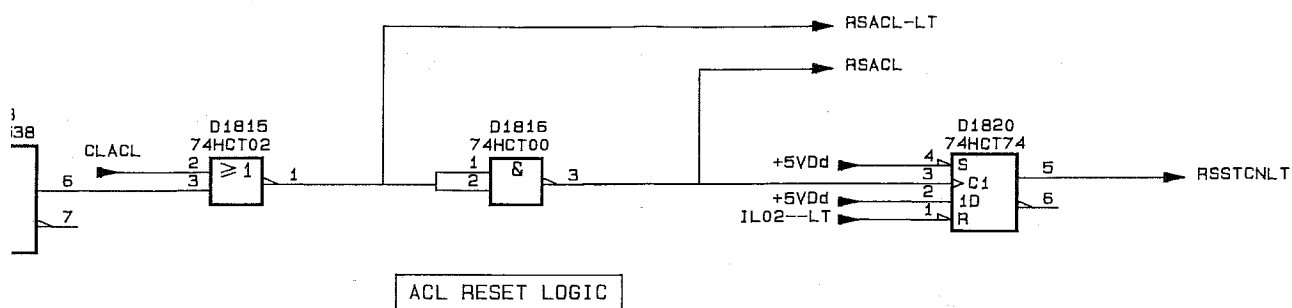
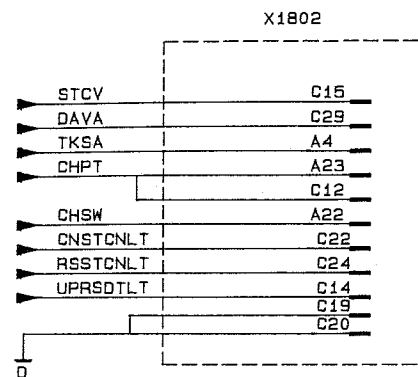


MAT3236

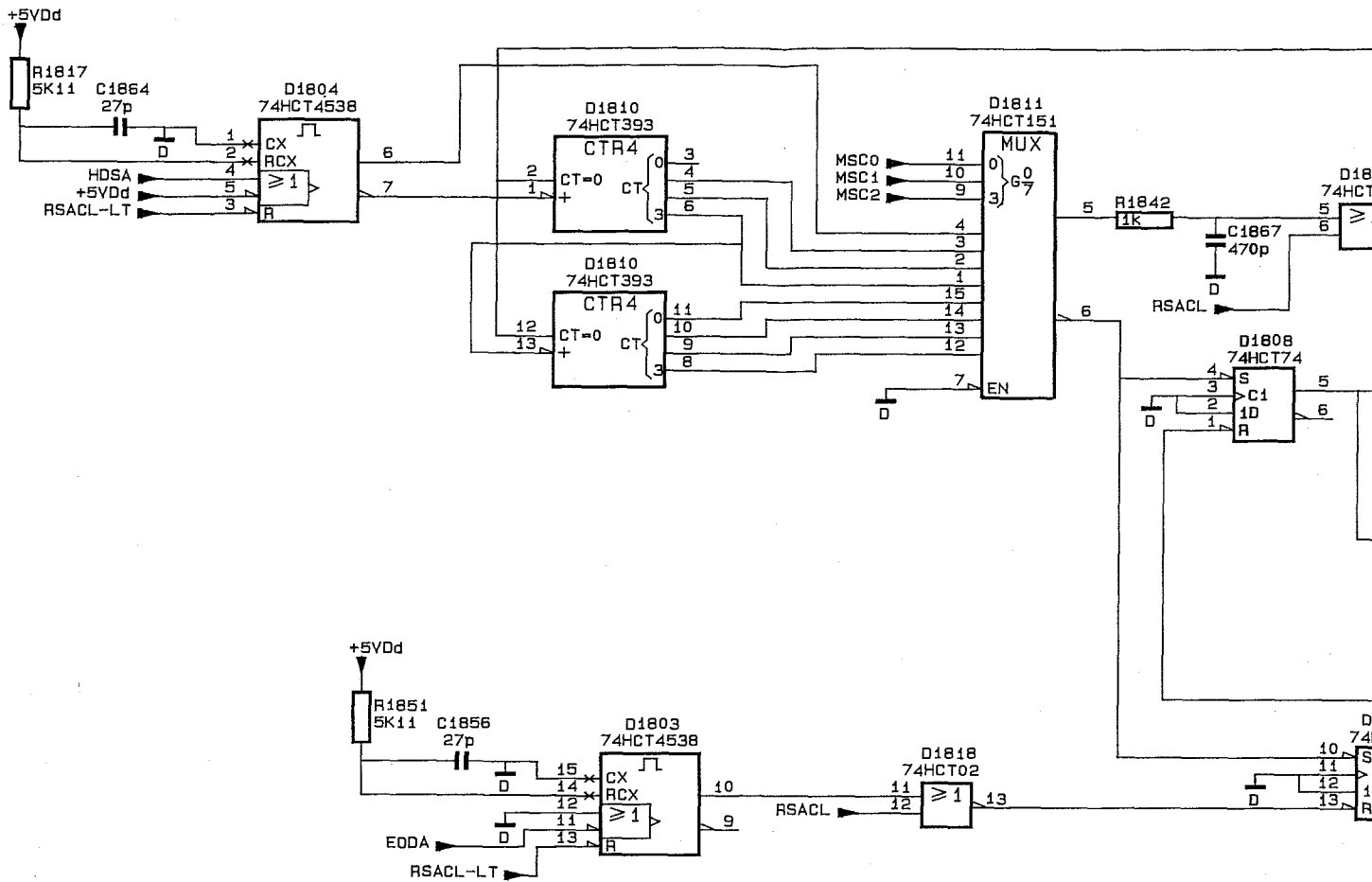
+5Vd _a	+5Vd _b	VBB _a	1
	20		10
	20		10
	20		10
20			10
20			10
14			7
14			7
14			7
		14	7
		28	14
		28	14
28			14
14	28		14
			7



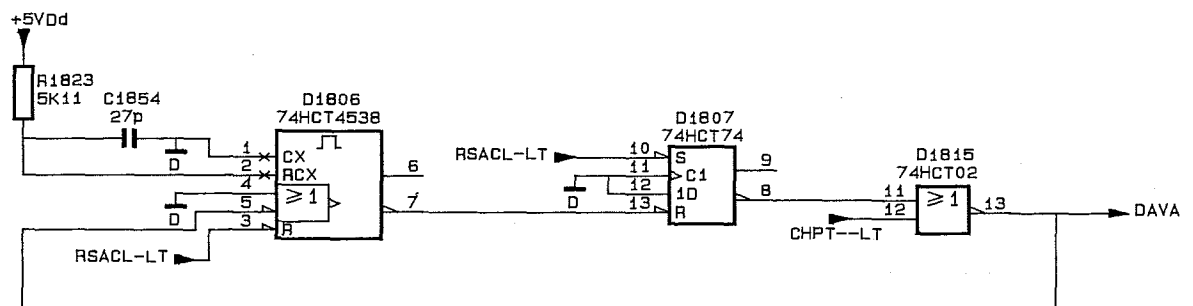
CLACL
 DUAL
 B
 A
 RSC2
 RSC1
 RSC0
 MSC2
 MSC1
 MSC0

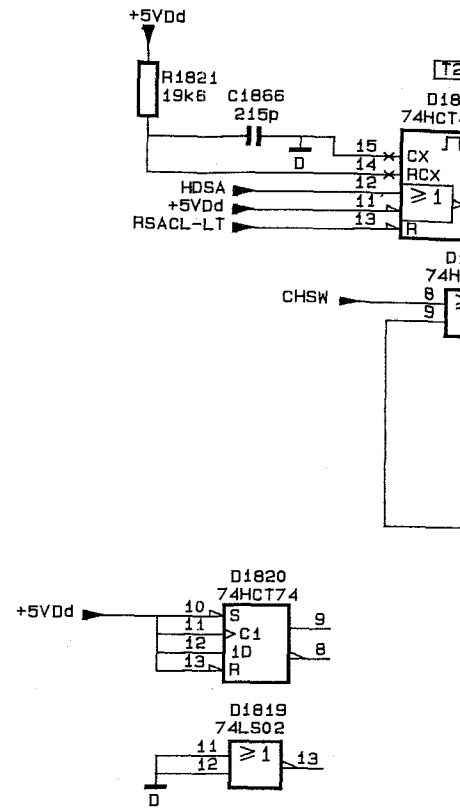
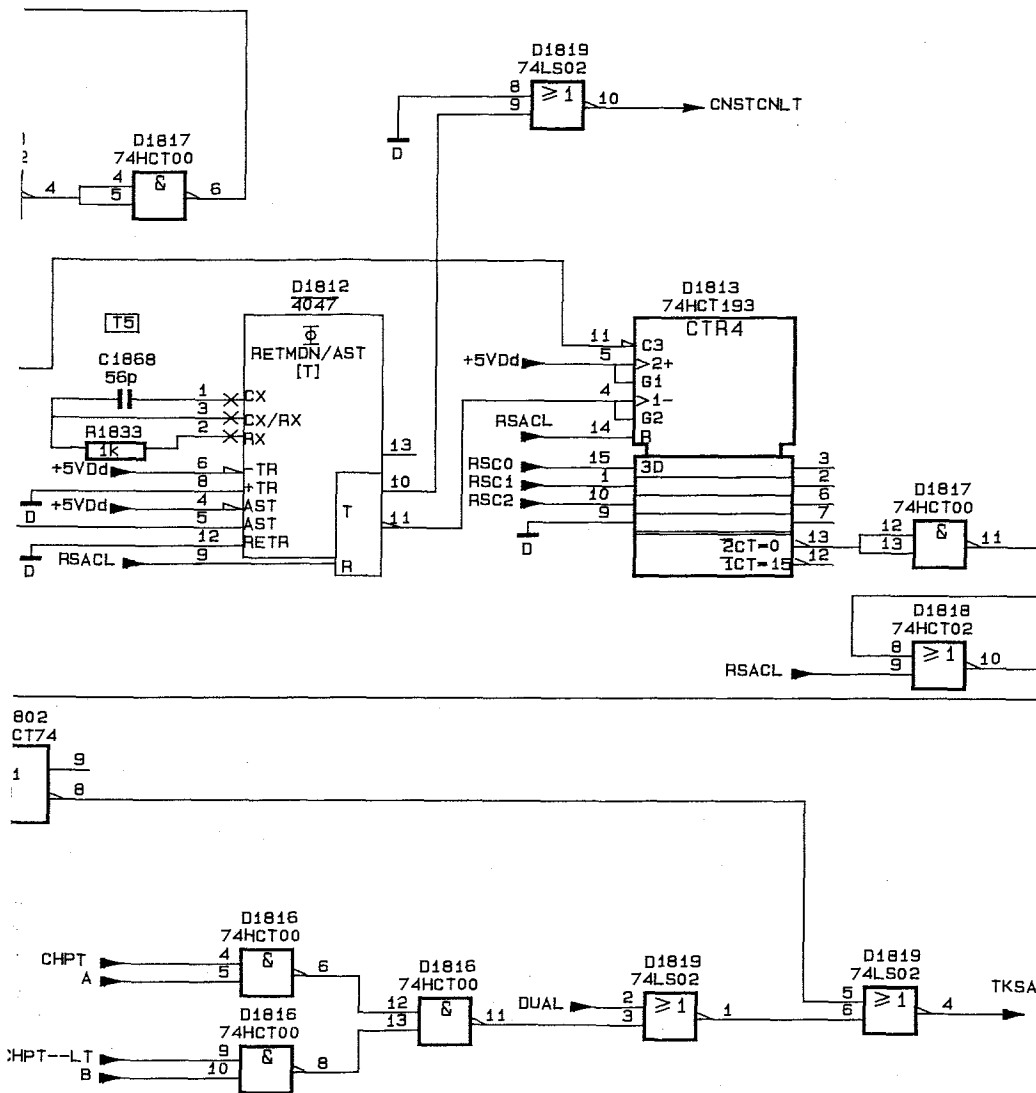


MAT3237



ACQUISITION CONTROL LOGIC

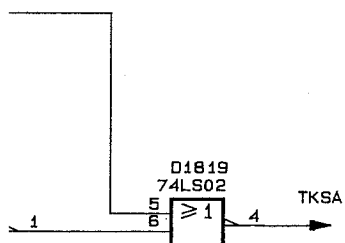
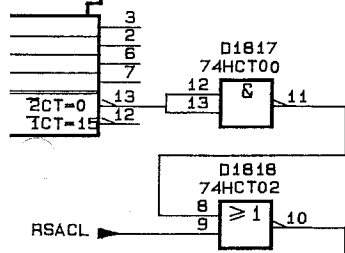




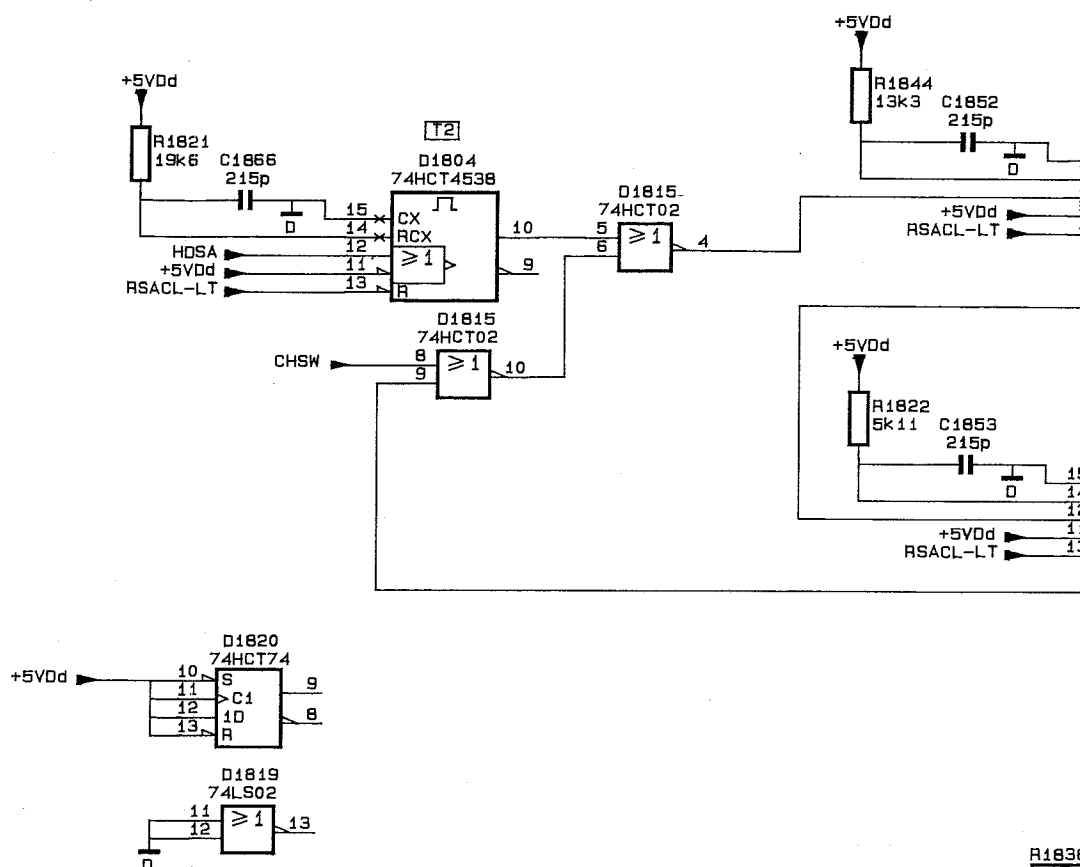
MAT3238

REFNR	TYPE	+5VdC	+5VdD
D1801	74HCT4538		16
D1802	74HCT74		14
D1803	74HCT4538		16
D1804	74HCT4538		16
D1805	74HCT4538		16
D1806	74HCT4538		16
D1807	74HCT74		14
D1808	74HCT74		14
D1809	74HCT74		14
D1810	74HCT393		14
D1811	74HCT151		16
D1812	HEF4047		14
D1813	74HCT193		16
D1814	TEA1017	7	
D1815	74HCT02		14
D1816	74HCT00		14
D1817	74HCT00		14
D1818	74HCT02		14
D1819	74LS02		14
D1820	74HCT74		14

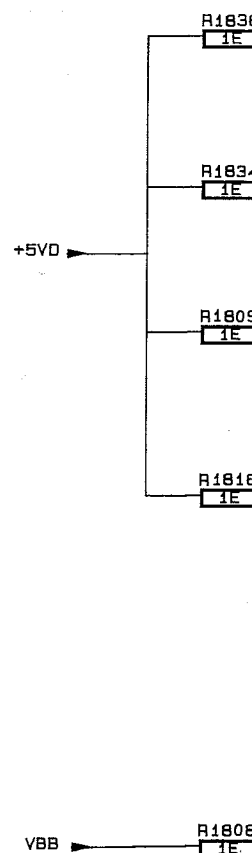
813
:T193
TR4



MAT3238



REFNR	TYPE	+5Vdc	+5Vdd	LD
D1801	74HCT4538		16	8
D1802	74HCT74		14	7
D1803	74HCT4538		16	8
D1804	74HCT4538		16	8
D1805	74HCT4538		16	8
D1806	74HCT4538		16	8
D1807	74HCT74		14	7
D1808	74HCT74		14	7
D1809	74HCT74		14	7
D1810	74HCT393		14	7
D1811	74HCT151		16	8
D1812	HEF4047		14	7
D1813	74HCT193		16	8
D1814	TEA1017	7		3
D1815	74HCT02		14	7
D1816	74HCT00		14	7
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D1818	74HCT02		14	7
D1819	74LS02		14	7
D1820	74HCT74		14	7



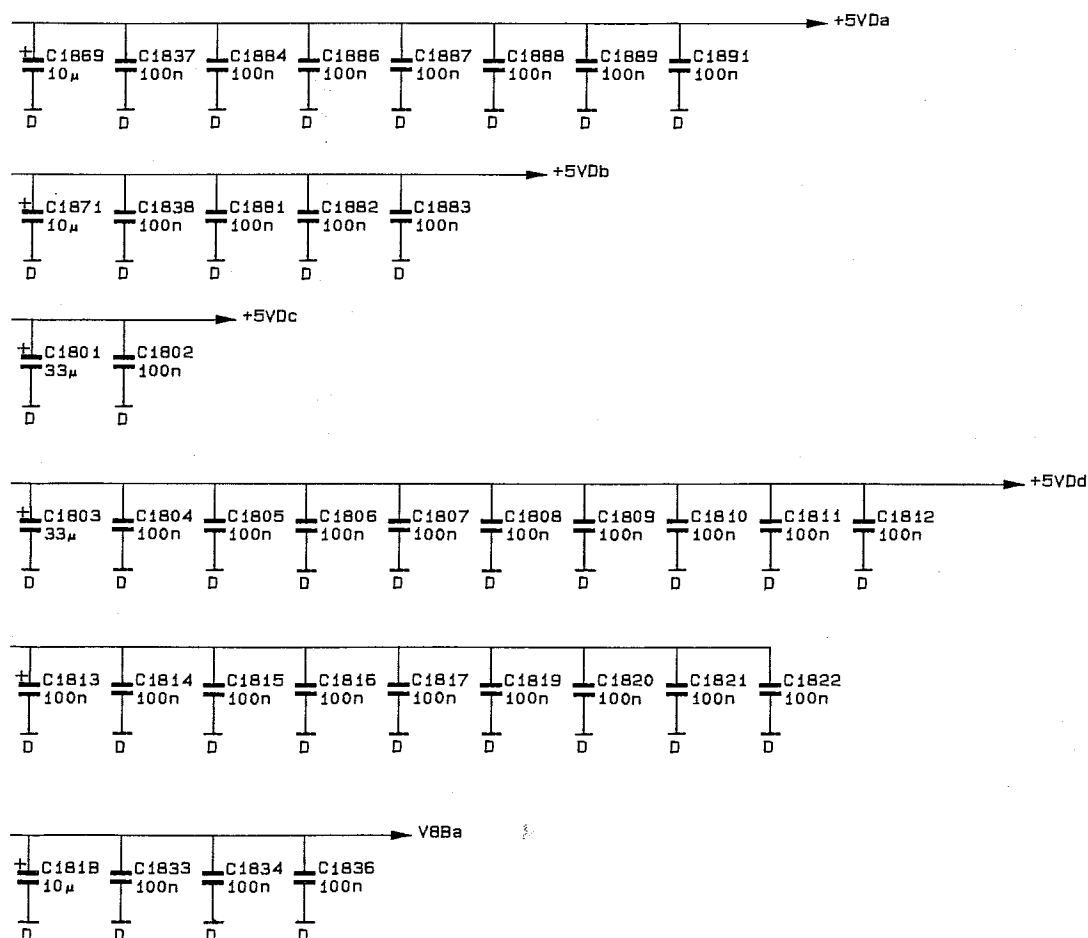
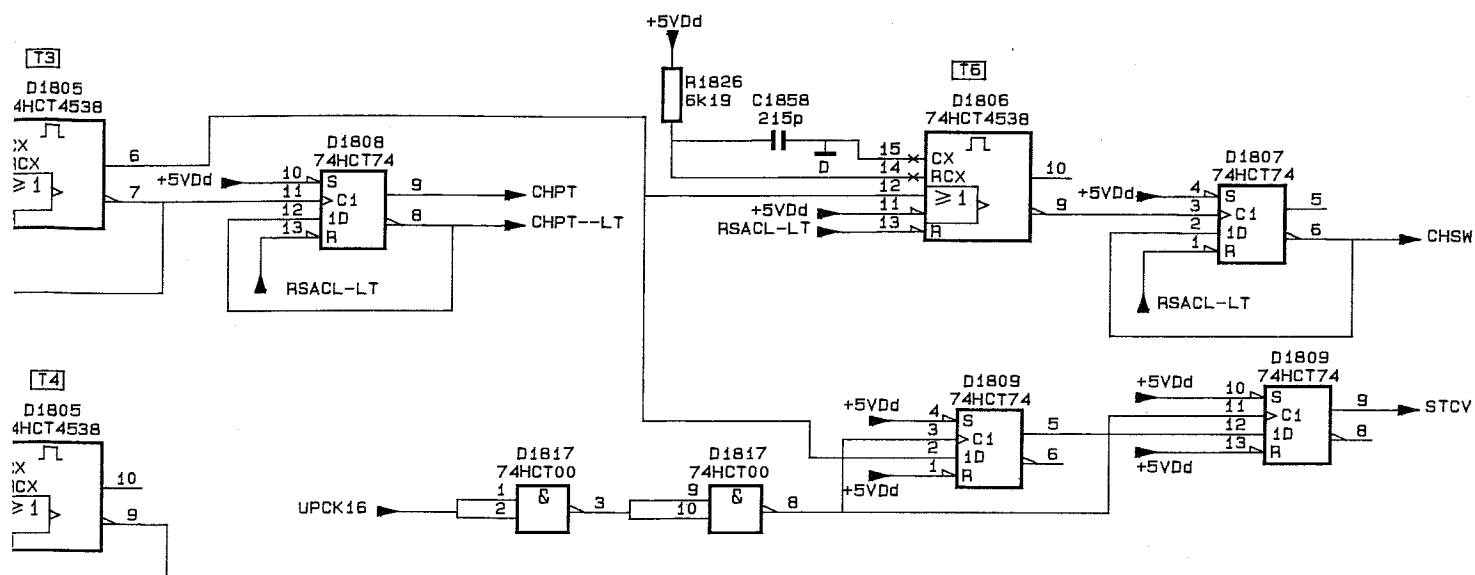


Figure 8.5.4 Unit A5 - GRAM UNIT - circuit diagram.