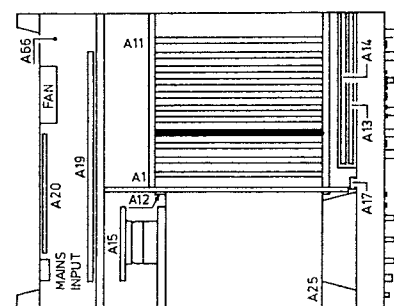


UNIT A4 - DISPLAY MEMORY UNIT

TOP VIEW

MAT3144

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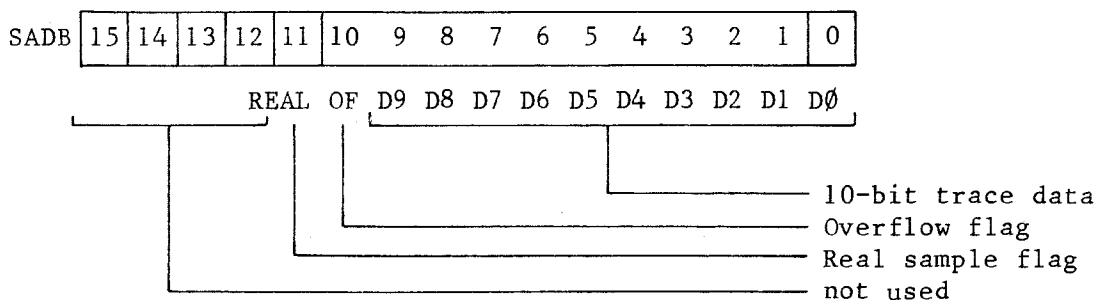
8.4.1 General information

This unit basically comprises the four random-access registers R0, R1, R2 and R3 of the trace memory, the text memory, the copy address counter and their associated control circuits.

8.4.2 Copying trace data from the DPU into display register R0

On receipt of a trigger pulse, a coupling is realized between the DPU (digital processing unit) and register R0 of the trace memory unit. The DPU places its 12-bit (two - complement) trace data on the sample data bus lines SADB00...SADB12. This bus is connected to the trace data latch consisting of D2001 and 2002. Each trace data word is clocked in the latch with signal latch enable display (LEDP). This is done in the rhythm of the acquisition system.

Trace data format:



Signal LEDP switches also a handshake flipflop D2017, resulting in an active SARY (sample ready) signal. When the trace data word is copied to register R0, the SARYAKLT signal resets the handshake flip flop, which informs the DPU that the next trace data word can be sent to the trace data latch.

In this way the display unit is informed that new trace data is available on the output bus lines TRDB00 ... TRDB15 of the trace data latch. This trace data bus is connected to the four display registers. New trace data however is always stored in register R0. This is done in a rhythm which is determined by the acquisition system.

RAM's D2008 and D2009 form together the two 4kx16 registers R0 and R1 and D2011 and D2012 form together the two 4kx16 registers R2 and R3.

Addresses for register R0 needed during the copy cycle of trace data from the DPU into register R0, are generated by a copy address counter which consists of D2018, D2019 and D2021.

The copy counter address bits CPAB00 ... CPAB11 are applied to the trace register R0 via address multiplexer II consisting of D2037, D2038 and D2039 as TRAB01 ... TRAB12.

Address line TRAB13 is separately generated and is used for the switching between R0 and R1 or between R2 and R3.

The counter is first resetted to its zero state by signal RSDU--LT (reset DPU). After an active trigger the copy cycle is started and the register will be completely filled once with trace data from the acquisition system. The counter is counting (and thus producing addresses for register R0. CNCPCN pulses (count pulses for the copy address counter) which are generated in the rhythm in which the acquisition system offers the new trace data. At the end of the copy cycle, the counter generates a signal TCCPCN (terminal count copy address counter) and the cycle is stopped.

Register R0 is furthermore controlled by its chip select signals CSTR1LLT and CSTR1HLT which can only be active when the memory select down signal MYSLDWLT is not active and by the write enable signal WETR01LT.

8.4.3 Saving trace data from register R0 into one of the registers R1, R2 or R3.

The address information needed for register R0 and the selected register is generated by the display address counter. The address lines DPAB00 ... DPAB11 are applied to the registers R0, R1, R2 and R3 via address multiplexer I consisting of D2031, D2033, D2032 and D2041 when cycle counter display address bus signal CLDPAB is active and via address multiplexer II consisting of D2037, D2038 and D2039 as TRAB0 ... TRAB12 when multiplexed copy address signal MXCPAD is active.

Each trace data word on the register R0 trace data output lines TRDB00...TRDB15 is first saved in a save latch consisting of D2028 and D2029 with the clock save latch signal CKSVLA.

The saved word is then afterwards saved in the selected memory by using exactly the same display address. Address line TRAB13 is switched to point to the selected register which is activated via its chip select signal and write enable signal.

The output of the save latch is disabled by the disable save latch signal DISVLA. For the next word the microprocessor increases the address number and so on. After 4096 of these actions the save action is completed. The save latch is not used when data has to be saved in register R2 or R3. Save is then done directly from R0 to R2 and to R3.

8.4.4 Storage of text in the text memory

All used kinds of texts are generated by the microprocessor system and stored when they are needed in a 8kx16 bit text memory consisting of D2014 and D2016.

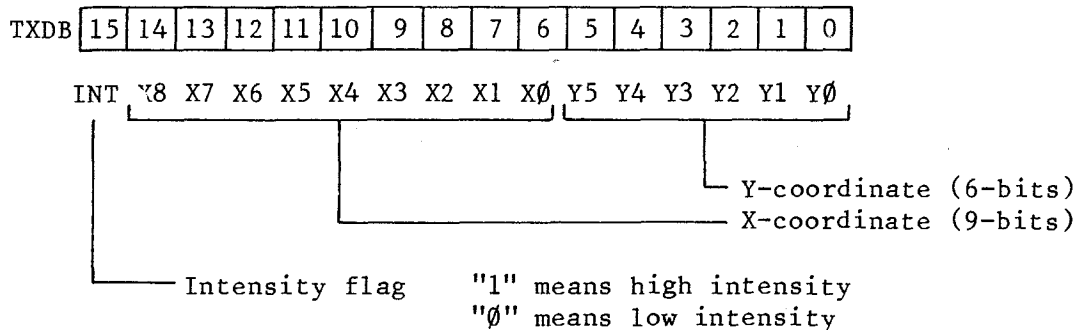
The addresses needed for the storage of text in the text memory are generated by the microprocessor. The microprocessor address lines AB01 ... AB12 are applied to the text memory via address multiplexer I consisting of D2031, D2032, D2033 and D2041 as TXAB01 ... TXAB12.

The text data consists of vertical and horizontal coordinates and an intensity flag. This data is generated by the microprocessor system. The data bits DB00 ... DB15 are applied via a bidirectional latch consisting of D2003 and D2004 as TXDB00 ... TXDB15 to the text memory.

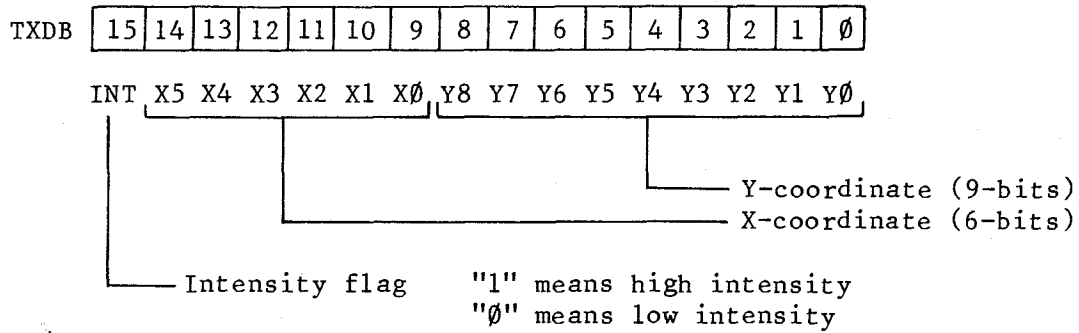


The following text data formats exist:

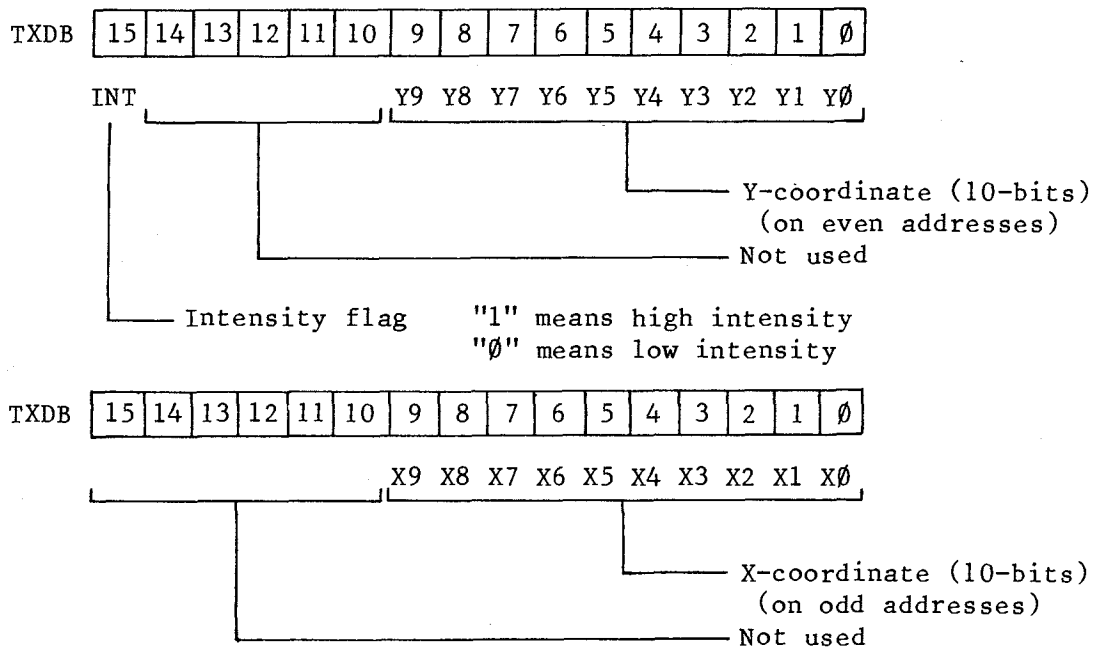
Top area text (TAT)
Trace area text (TRAT)
Bottom area text (BAT)



Softkey text (SKT)



Miscellaneous text (MSC)



For storage of miscellaneous texts, two words are stored, one for the Y-coordinate and the intensity flag and the other one for the X-coordinate.

If no text has to be displayed, a word of only one's will be stored in the text memory and the trace will be suppressed.

8.4.5 Reading trace data for display purposes

The display memory addresses which are needed during the display cycle for trace data are generated by a display address counter which is located on the display control unit A3.

The display counter output address bits DPAB00 ... DPAB11 are applied via address multiplexer I and address multiplexer II to the address inputs of the four display registers R0, R1, R2 and R3.

Each register can be selected for display by the generation of its chip select signal, its output enable signal and the register select signal TRAB13.

The selected register places its output data word on the trace data bus lines TRDB00 ... TRDB15. This data is applied to the display control latch by latch enable display control latch signal LEDC. The output data bits DCDB00 ... DCDB15 are applied then to the display DAC unit A2 for further handling.

8.4.6 Reading text data for display purposes

The text memory addresses which are needed during the display cycle for text data are generated by the display address counter. These display address counter address bits DPAB00 ... DPAB11 are applied via address multiplexer I to the address inputs of the text memory. The text memory is selected by the generation of its chip select signal, its output enable signal and the register select signal TXAB13. The text output data word is placed on the text data bus lines TXDB00 ... TXDB15 and via the text/trace buffer consisting of D2006 and D2007 applied to the display control latch. The output data bits DCDB00 ... DCDB15 are applied then to the display DAC unit A2 for further handling.

8.4.7 Data communication via options

Instruments which are equipped with option can communicate with the trace memory as well as the text memory via the following signal paths.

Trace memory:

Addresses are generated by the microprocessor and via address multiplexers I and II applied to the display memory. Data communication is done via the microprocessor data bus, the bidirectional text/trace buffer and the trace data bus or vice versa.

Text memory:

Addresses are generated by the microprocessor and via address multiplexer I applied to the text memory. Data communication is done via the microprocessor bus, the bidirectional data/text latch and the text data bus or vice versa.

8.4.8 Trigger address comparator

The TRIGGER ADDRESS COMPARATOR is part of the address generator on the DPU CONTROL (Unit A8).

It has no function in this instrument.

8.4.9 Signal name list

UNIT A4

Signal name	Description	Signal source	Signal destination(s)
AB01...12	Address bus 01...12	A6+option	-
CKSVLA	Clock save latch	A3	-
CLDPAB	Clock display address bus	A3	-
CLUPAB	Clock microprocessor bus	A3	-
CNCPCN	Count copy address counter	A8	-
CPAB00...11	Copy counter address bus 00...11	A4	A4
CSTR1LLT	Chip select trace 1L	A4	A4
CSTR1HLT	Chip select trace 1H	A4	A4
CSTR2LLT	Chip select trace 2L	A4	A4
CSTR2HLT	Chip select trace 2H	A4	A4
CSTX--LT	Chip select text	A3	-
DAAK--LT	Data acknowledge	A3	-
DAAK--HT	Data acknowledge	A3	-
DAVA	Data valid	A5	-
DB00...15	Data bus 00...15	A6+option	-
DCDB00...15	Display control data bus 00...15	A4	A12-A2, A12-A3
DIDBTX	Disable data bus text-buffer	A3	-
DIDCLA	Disable display control latch	A4	-
DISVLA	Disable save latch	A3	-
DITRDB	Disable trace data bus (SARYAKLT)	A3	-
DITXTR	Disable text trace buffer	A3	-
DPAB00...11	Display address bus 00...11	A3	-
DRTXTR	Direction text trace buffer	A3	-
DUAB00...11	DPU address bus 00...11	A8	-
ENCPSA	Enable copy sample	A4	A12-A8
LEDC	Latch enable display control	A3	-
LEDP	Latch enable display	A8	-
MXCPAD	Multiplex copy address	A3	-
MYSLDWLT	Memory select down	A6	-
MYSL02LT	Memory select 02	A6+Option	-

Signal-name	Description	Signal source	Signal destination(s)
OETR01LT	Output enable trace 01	A3	-
OETR02LT	Output enable trace 02	A3	-
OETX--LT	Output enable text	A3	-
OFDP	Overflow display	A9	-
OTCM	Output comparator	A4	A12-A8
RDDM--LT	Read display memory	A3	-
RLDP	Real sample display	A9	-
RSDU--LT	Reset DPU	A8	-
SADB00...09	Sample data bus 00...09	A9+A11	-
SARY	Sample ready	A4	A3
SARYAKLT	Sample ready acknowledge (DITRDB)	A3	-
SLTR1LLT	Select trace 1L	A3	-
SLTR1HLT	Select trace 1H	A3	-
SLTR2LLT	Select trace 2L	A3	-
SLTR2HLT	Select trace 2H	A3	-
TCCPCN	Terminal count copy address counter	A4	A12-A8
TRAB01...12	Trace address bus 01...12	A4	A4
TRAB13	Trace address bus 13	A3	-
TRDB00...15	Trace data bus 00...15	A4	A4
TXAB01...12	Text address bus 00...12	A4	A4
TXAB13	Text address bus 13	A3	-
TXDB00...15	Text data bus 00...15	A4	A4
UPCK08	Microprocessor clock 8 MHz	A6	-
WETR01LT	Write enable trace 01	A3	-
WETR02LT	Write enable trace 02	A3	-
WETX--LT	Write enable text	A3	-

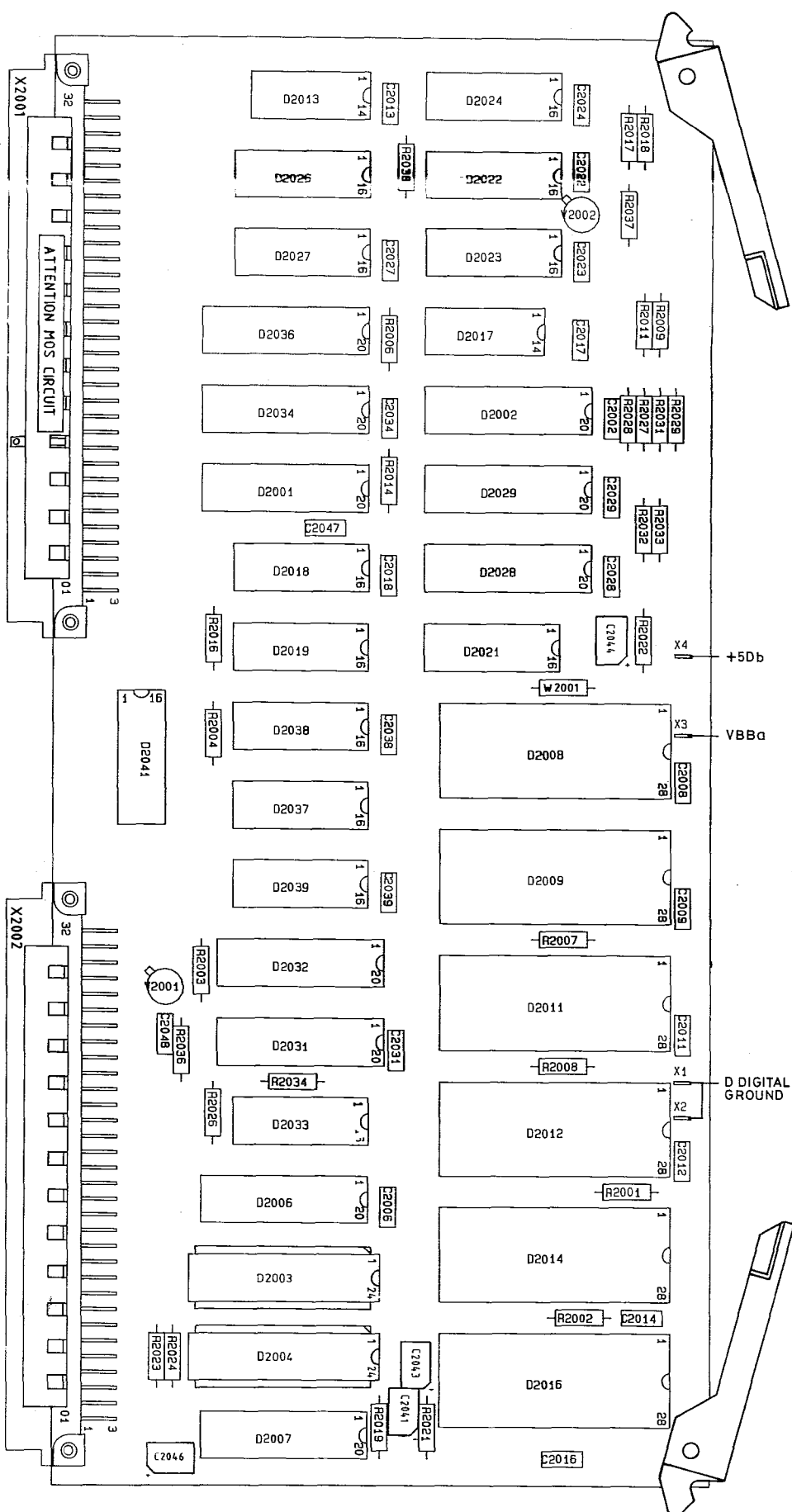


Figure 8.4.1 Unit A4 - DISPLAY MEMORY UNIT - p.c.b. lay-out.

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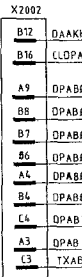
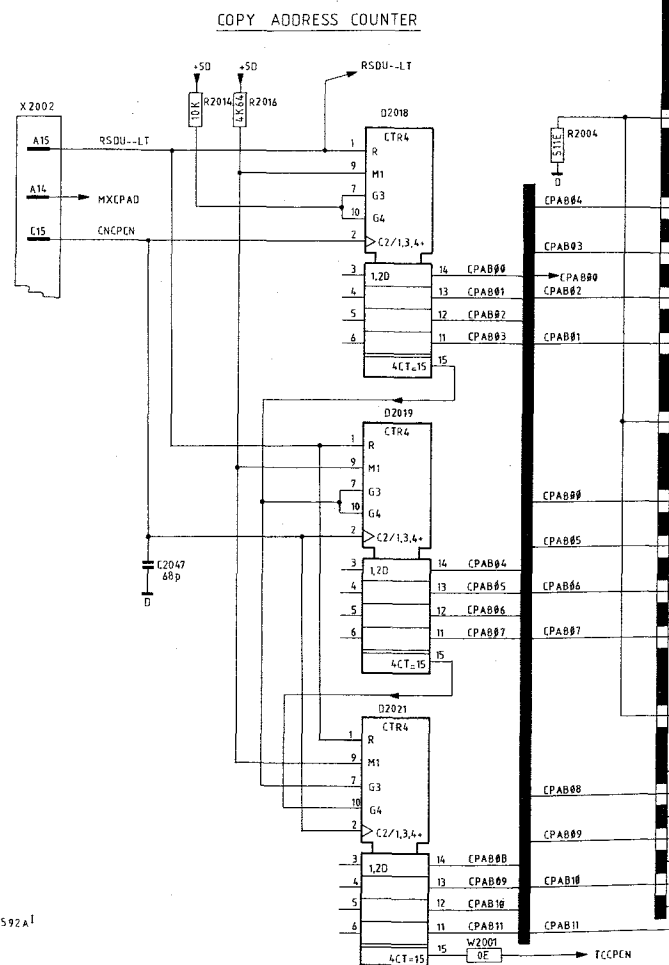
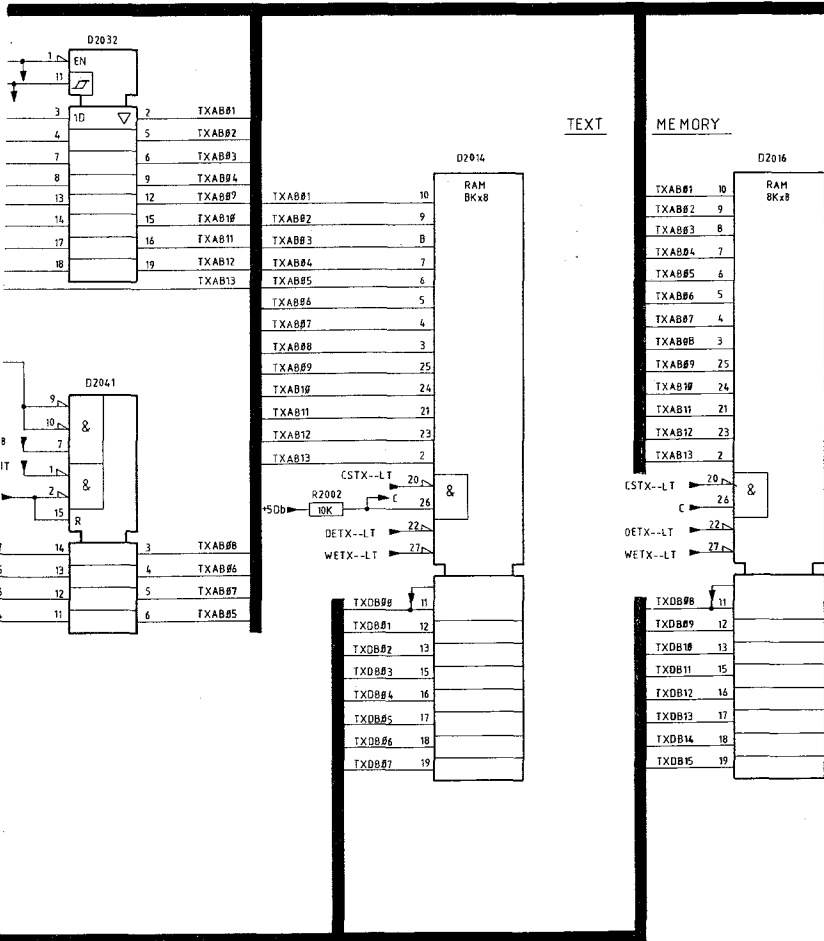
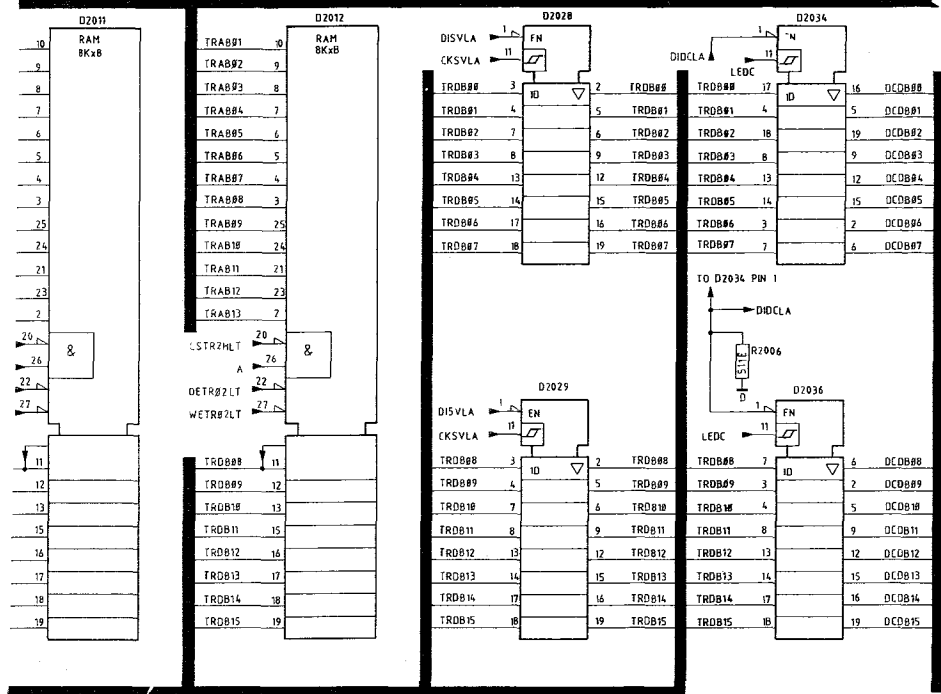


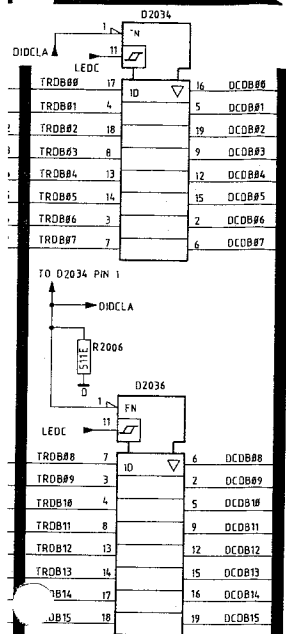
Figure 8.4.2 Unit A4 - DISPLAY MEMORY UNIT - circuit diagram.

Y
R2 - R3
SAVE LATCH
DISPLAY CONTROL LATCH



MAT 2592A1

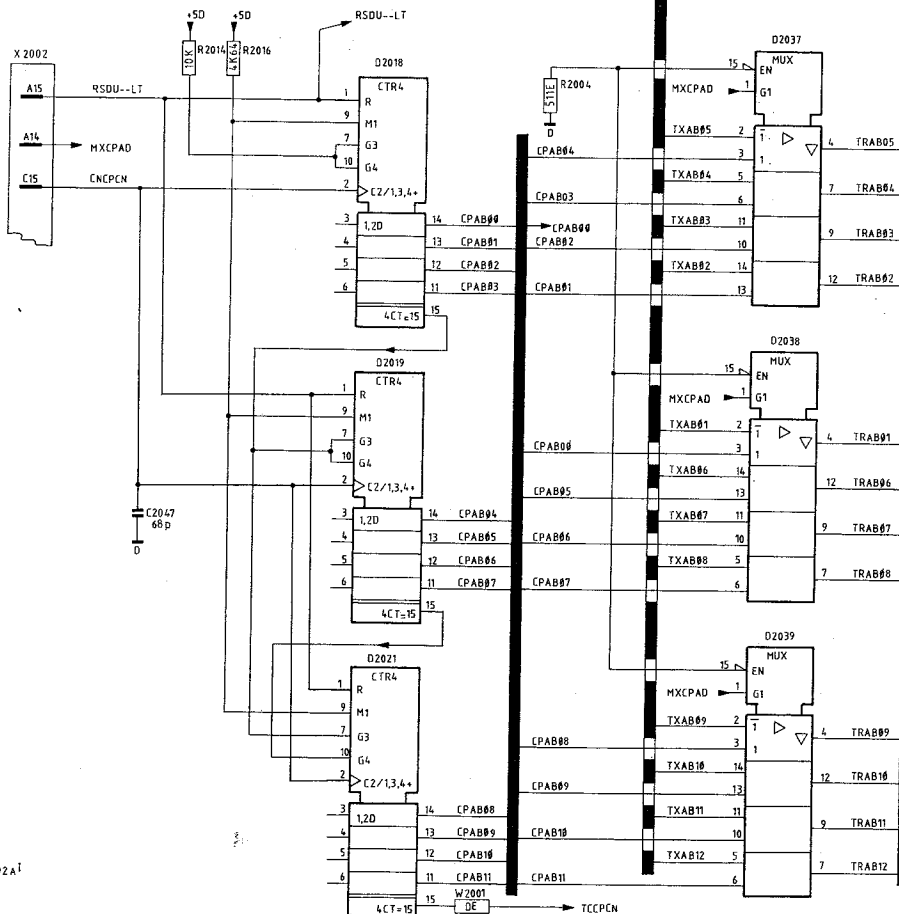
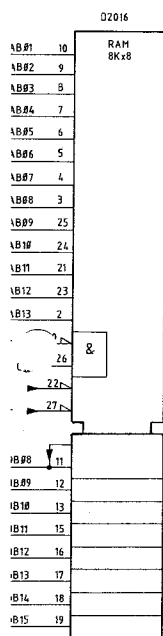
DISPLAY CONTROL LATCH



COPY ADDRESS COUNTER

ADDRESS MUX II

MEMORY



MAT 2592A1

