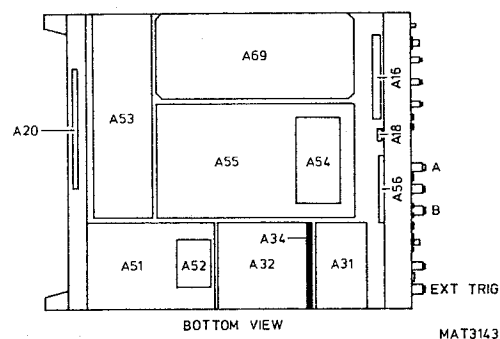


UNIT A34 TRIGGER CONTROL UNITCONTENTS

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8.34.1 General information

This unit controls the various trigger modes in this instrument, as well in manual select as in auto select mode. Furtheron, this unit contains a trigger level adaption circuit, which is switched between the Management unit and the Three Stage Trigger unit.

8.34.2 Principle of operation

Figure 8.34.1 shows the principle of operation of the trigger control.

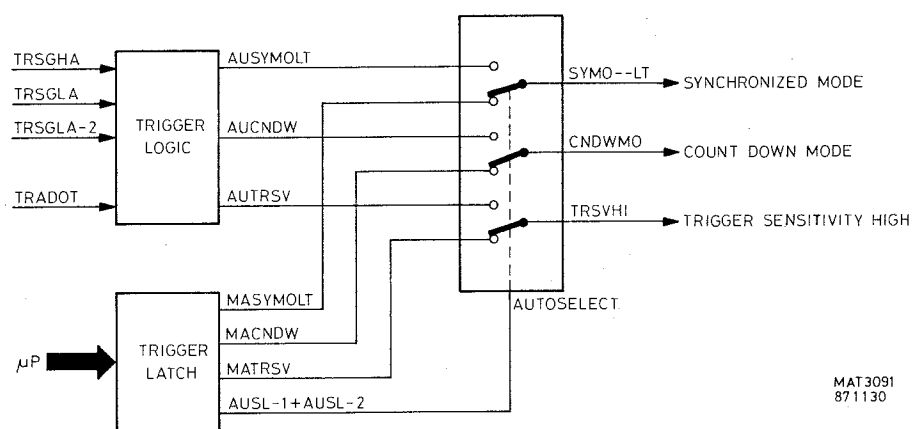
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Figure 8.34.1 Principle of trigger control.

Three signals (SYMO--LT, CNDWMO, TRSVHI) control the trigger mode. If AUTO SELECT is not selected, the switch, which is a multiplexer, is in the drawn position. The trigger mode is now determined by the signals from the microprocessor: MASYMOLT, MACNDW and MATRSV.

If AUTO SELECT is selected, the multiplexer is changed over by the microprocessor via the AUSL-1 and AUSL-2 signals. Now the trigger mode is determined by the AUSYMOLT, AUCNDW and AUTRSV signals, which come from the trigger logic.

To detect the desired trigger mode, depending upon the input signal of the instrument, the trigger logic gets 3 signals from Three Stage Trigger unit A32 (TRSGHA, TRSGLA and TRSGLA-2) and the TRADOT signal from the Trigger Input unit A31.

8.34.3 Circuit description

The trigger logic consists of the UPPER FREQUENCY DETECTOR, THE LOWER FREQUENCY DETECTOR, the TRIGGER MODE CONTROL and the COUNTDOWN CONTROL. If TRIGGER SENSITIVITY HIGH is selected and the input signal has a level of more than 10 mV, then the signal TRSGLA-2 is a square wave with the frequency of the input signal, divided by 32.

In TRIGGERED mode, the signal ENUFD (D2217 pin 6 and D2209 pin 1) is high, so the signal TRSGLA-2 is divided by 25 by the dividers in IC D2211.

So the frequency at pin 9 of D2211 is the frequency of the input signal, divided by 800 (32×25). This signal is applied to the UPPER FREQUENCY DETECTOR. This circuit consists of three monostable multivibrators and some logic. Each monostable multivibrator generates a pulse on its activating edge. If the frequency of the input signal passes above 160 MHz, the signal AUCNDW at pin 3 of D2204 goes high. The frequency determinating elements are C2242, R2212 and R2220. With the latter the frequency limit can be adjusted.

In COUNT DOWN mode the signal TRSGLA-2 is a square wave with the frequency of the input signal divided by 4096. In this mode the signal ENLFD (D2217 pin 5 and D2209 pin 4) is high, so the signal is applied to the LOWER FREQUENCY DETECTOR. This circuit is built up in a similar way as the UPPER FREQUENCY DETECTOR.

If the frequency of the input signal goes below 150 MHz, the signal AUCNDW at pin 3 of D2204 goes low. The frequency determinating elements are C2246, R2216 and R2225. With the latter the frequency limit can be adjusted.

The AUCNDW signal is applied to the COUNT DOWN CONTROL. Depending on the status of AUSL-2 the signal MACNDW or AUCNDW determines CNDWMO. Via transistor V2202, the PRESCALER on the Trigger Input unit A31 is activated in COUNT DOWN mode.

In AUTO SELECT mode, the instrument automatically switches over to COUNT DOWN mode if the frequency of the input signal passes above 160 MHz and switches back if the frequency passes below 150 MHz.

Because the sensitivity in COUNT DOWN mode is lower due to the PRESCALER on the Trigger Input unit A31, there might be no more trigger signal detected (no square wave at TRSGLA-2). Next the instruments switches back to TRIGGERED mode; detects a too high frequency, switches back to COUNT DOWN mode, etc.

This unstable situation is prevented by the circuit around gate D2208 (pin 8, 9 and 10), transistor V2211 and flipflop D2206.

If the instrument switches back to TRIGGERED mode, the flipflop is set and the DICNDWLT signal prevents via D2204 pins 13, 11, 1, 2 and 3 that AUCNDW goes high again. The flipflop is reset via the signal AUSL-2 if AUTO SELECT is deselected or selected again.

The TRIGGER mode control detects if TRIGGERED mode or SYNCHRONIZED mode should be selected in AUTO SELECT mode, depending on the frequency of the input signal. It also detects if the TRIGGER SENSITIVITY should be HIGH or LOW.

If the input signal has a level of more than 10 mV then TRSGLA is a square wave. If the level rises above 20 mV, TRSGHA is also a square wave. In both situations TRIGGER SENSITIVITY is assumed to be HIGH. If SYMO--LT is low, the signal TRSGHA passes via D2207 pins 12 and 11, else TRSGLA passes via D2202 pins 2 and 3. The following circuit detects if a square wave is present at D2212 pin 3, which results in the signals AUTRSV and AUSYMOLT.

Depending on the status of AUSL-1, the signal MATRSV or AUTRSV determines TRSVHI. Via transistor V2201, the X1/X10 AMPLIFIER on the Trigger Input unit A31 is activated if TRSVHI is high.

The signal AUSL-1 also determines if SYMO--LT is determined by MASYMOLT or AUSYMOLT.

The TRIGGER LATCH is a shift register, which latches a number of trigger status signals, which come from the microprocessor via the Management unit A25.

The TRIGGER LEVEL ADAPTION buffers the trigger level current from the MANAGEMENT unit A25. The output current is applied to the Three Stage Trigger unit A32. With potentiometer R2232, the trigger level offset can be adjusted.

8.34.4 Signal name list

UNIT 34

Signal name	Description	Signal source	Signal destination(s)
AUCNDW	Auto count down mode	A34	A34
AUSL-1	Auto select 1	A34	A34
AUSL-2	Auto select 2	A34	A34
AUSYMOLT	Auto synchronized mode	A34	A34
AUTRSV	Auto trigger sensitivity	A34	A34
CNDWMO	Count down mode	A34	A34, A51-A53-A25
CNDWMOLT	Count down mode	A34	A31
DICNDWLT	Disable count down	A34	A34
ENLFD	Enable lower frequency detector	A34	A34
ENPS--LT	Enable prescaler	A34	A32
ENUFD	Enable upper frequency detector	A34	A34
ETTR	External triggering	A34	A31
LETRST	Latch enable trigger status	A25	-
MACNDW	Manual count down	A34	A34
MASYMOLT	Manual synchronized mode	A34	A34
MATRSV	Manual trigger sensitivity	A34	A34
SECK1	Serial clock 1	A25	-
SEDA1	Serial data 1	A25	-
SYMO--LT	Triggered mode	A34	A32,A51, A51-A53-A25
TR-A	Triggering channel A	A34	A31
TR-B	Triggering channel B	A34	A31
TRADOT	Trigger amplitude detector output	A32	-
TRLV	Trigger level	A34	-
TRLV-1	Trigger level 1	A34	A32
TRMORSLT	Trigger mode reset	A34	A34
TRSGHA	Trigger signal high amplitude	A32	-
TRSGLA	Trigger signal low amplitude	A32	-
TRSGLA-2	Trigger signal low amplitude 2	A32	-
TRSP	Trigger slope	A34	A32
TRSVHI	Trigger sensitivity high	A34	A51-A53-A25
TRSVHILT	Trigger sensitivity high	A34	A31

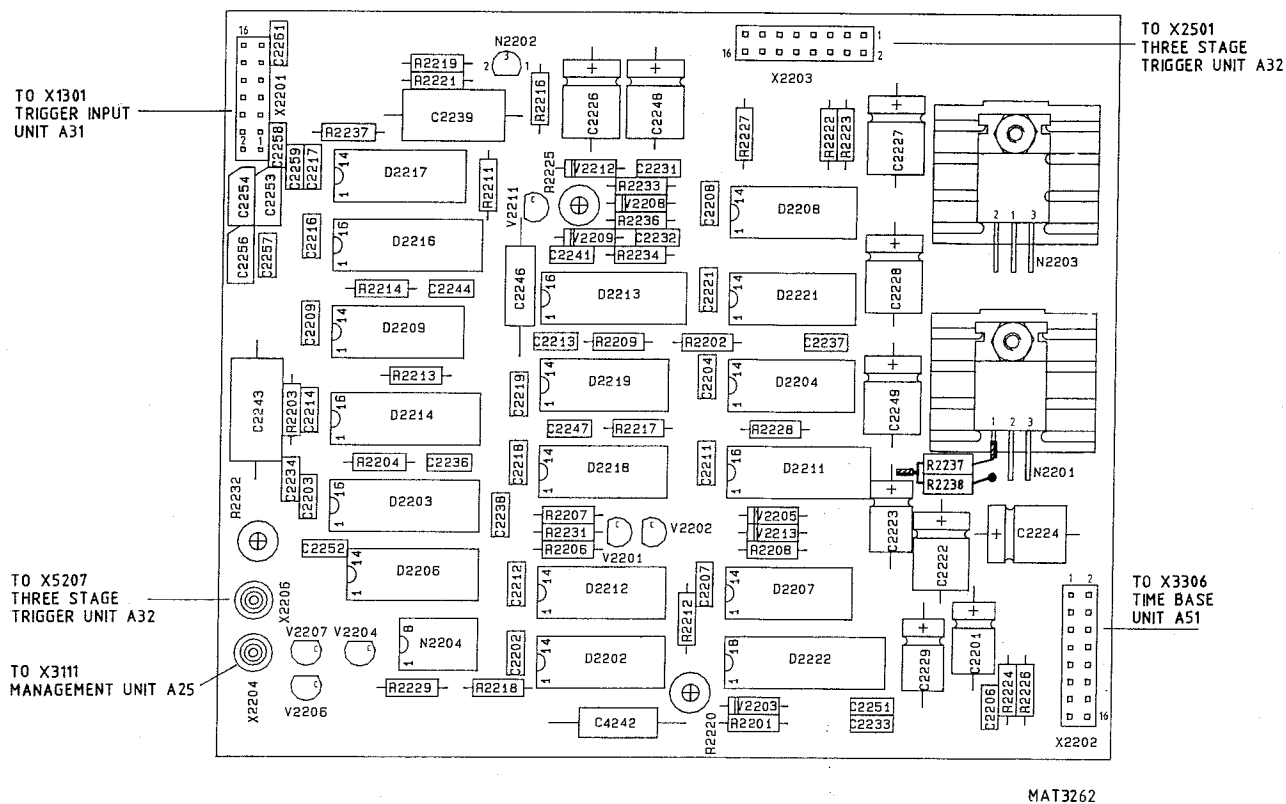


Figure 8.34.2 Unit A34 - TRIGGER CONTROL UNIT - p.c.b. lay-out.

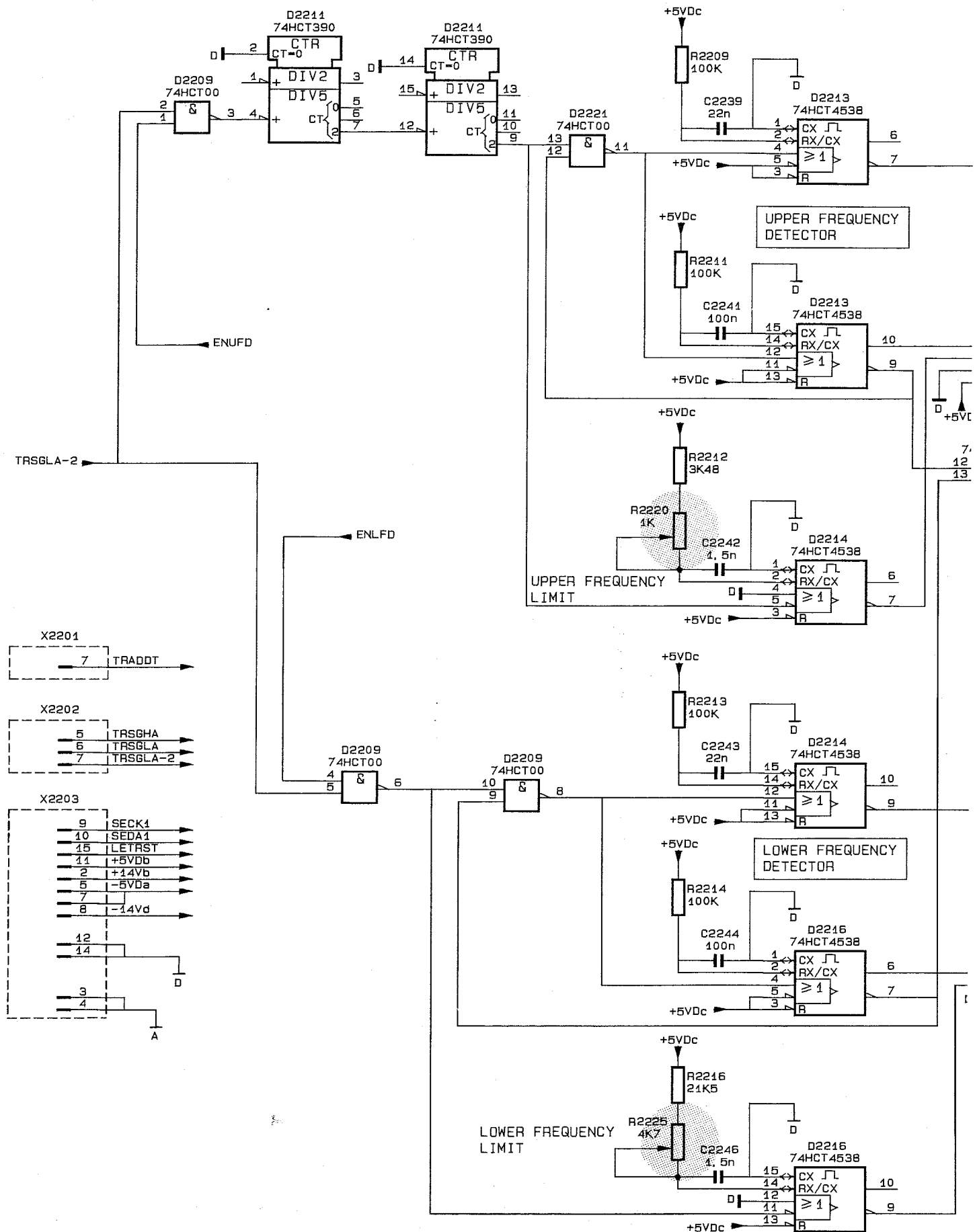
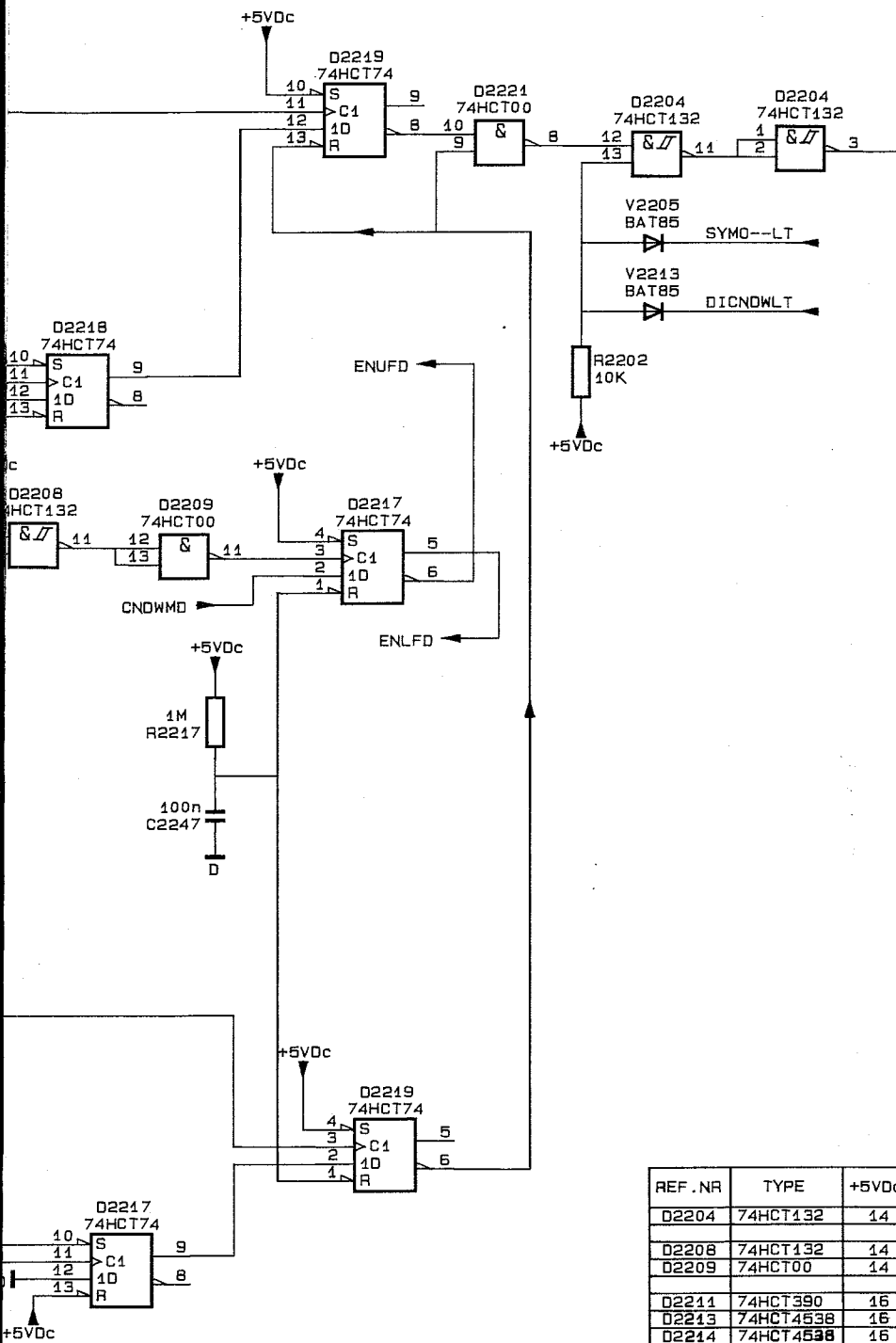
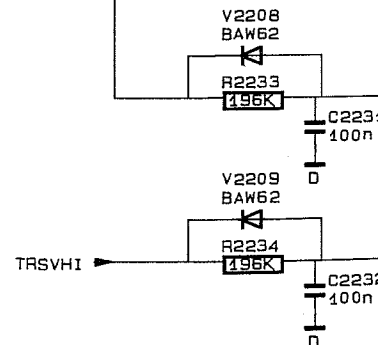
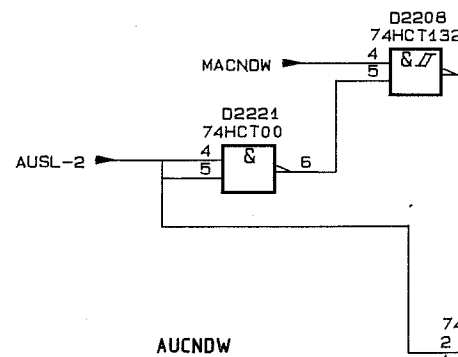
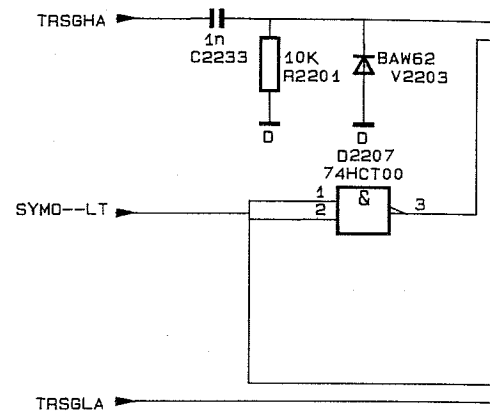


Figure 8.34.3 Unit A34 - TRIGGER CONTROL UNIT - circuit diagram.

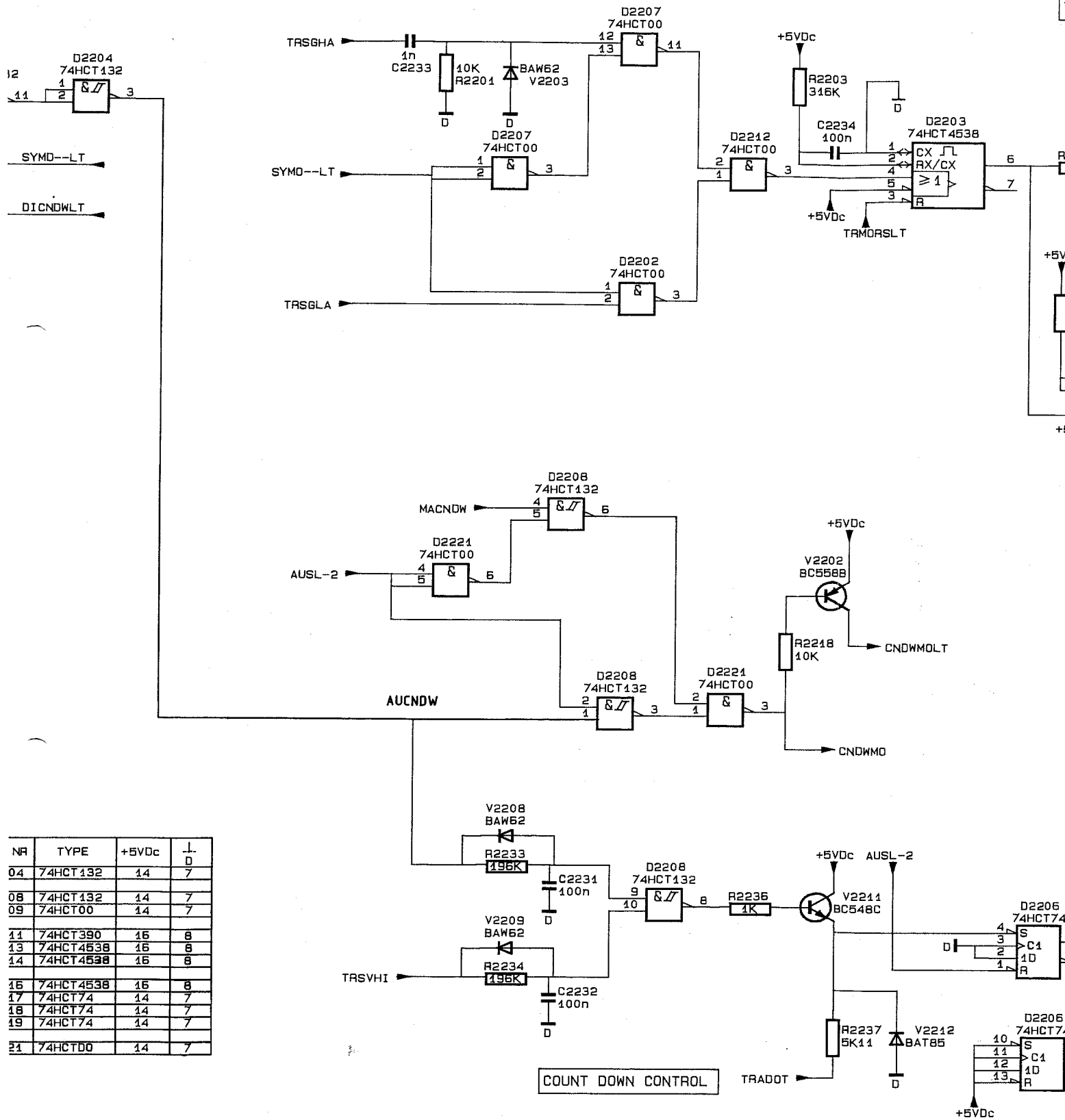


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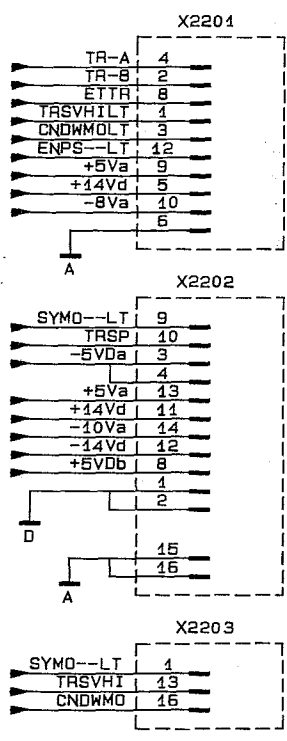
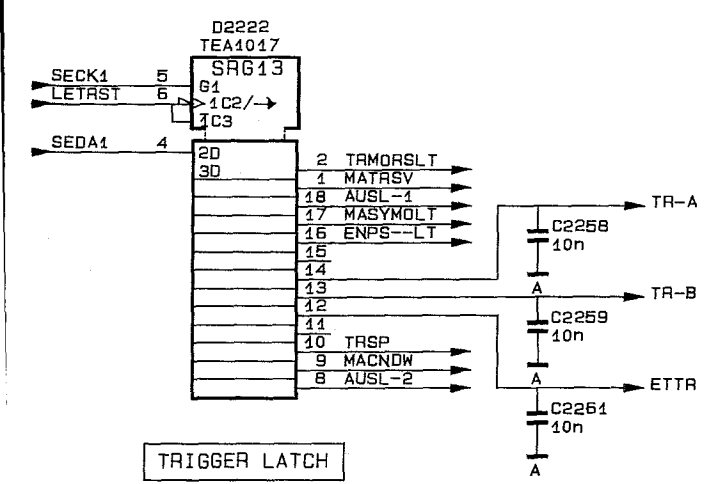
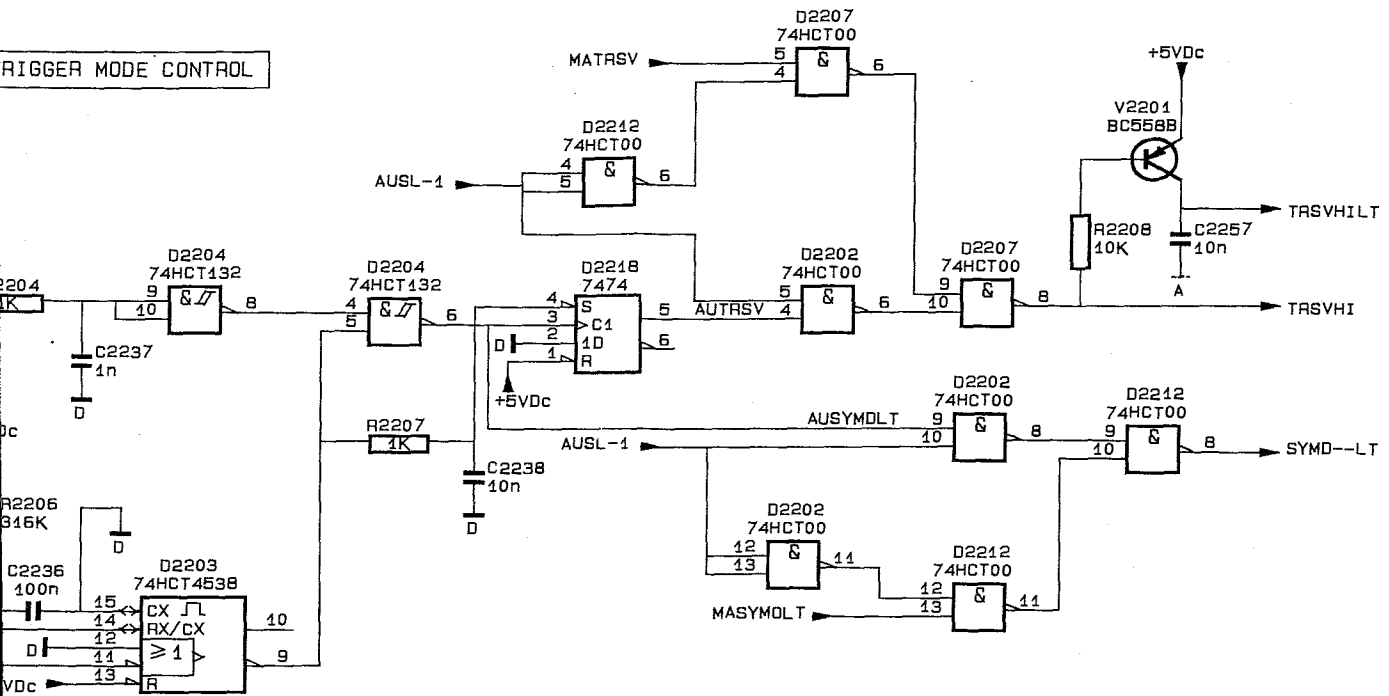
REF. NR	TYPE	+5VDC	I/O
D2204	74HCT132	14	7
D2208	74HCT132	14	7
D2209	74HCT00	14	7
D2211	74HCT390	16	8
D2213	74HCT4538	16	8
D2214	74HCT4538	16	8
D2216	74HCT4538	16	8
D2217	74HCT74	14	7
D2218	74HCT74	14	7
D2219	74HCT74	14	7
D2221	74HCT00	14	7



COUNT



RIGGER MODE CONTROL

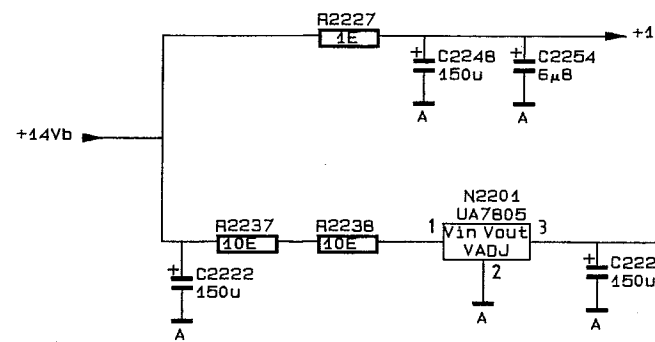
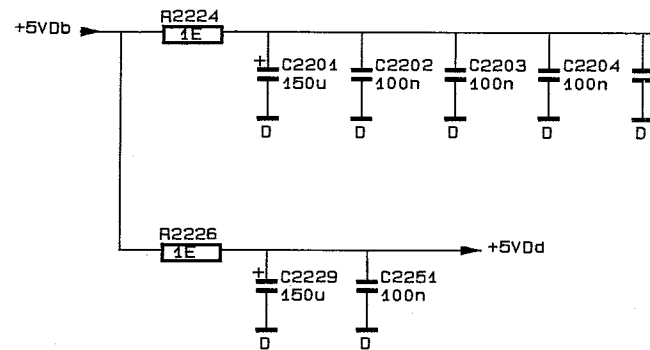
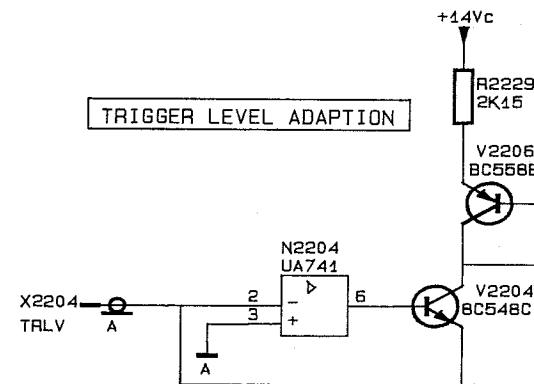


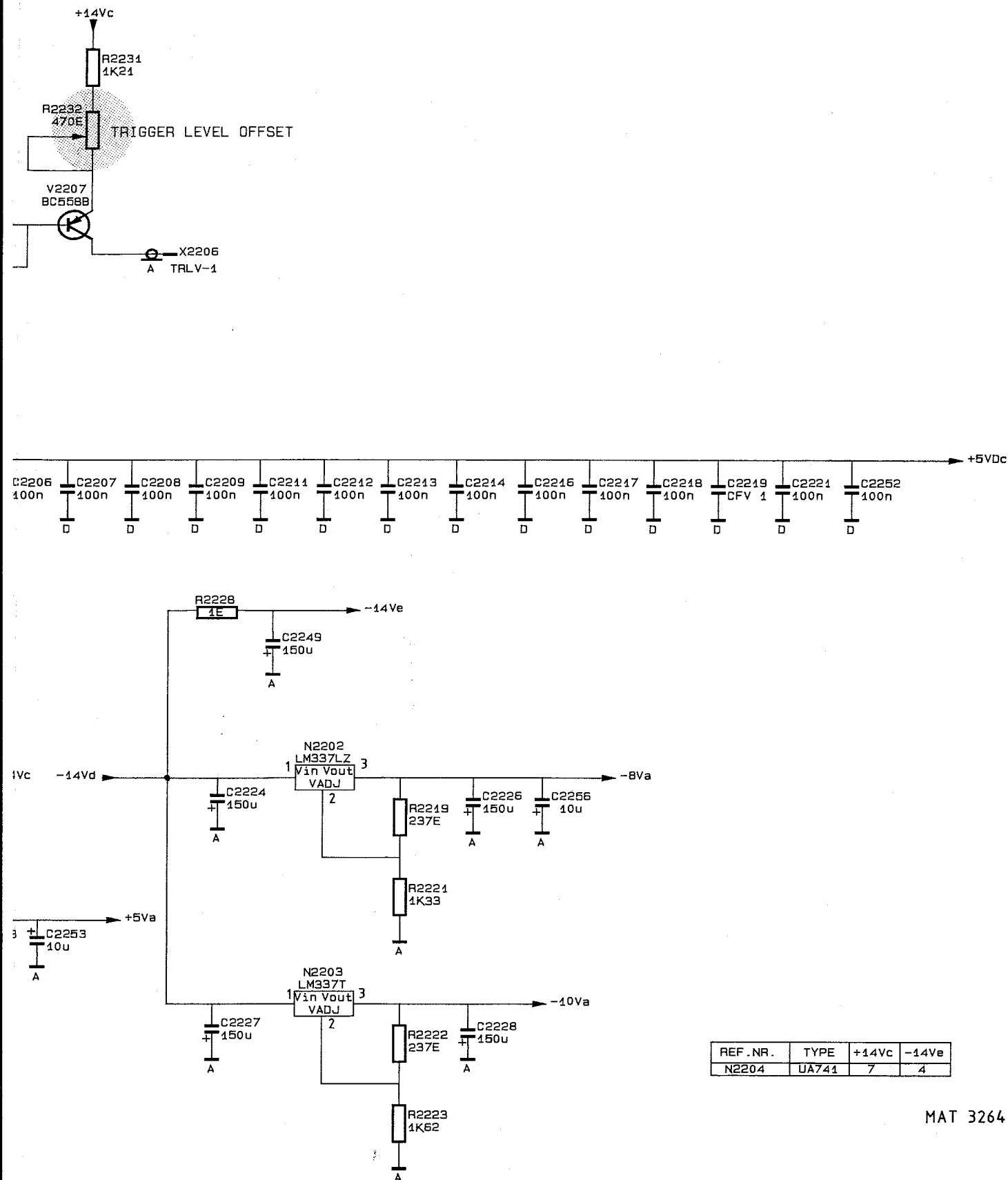
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5
6 → DICNDWLT

REF.NR	TYPE	+5Vdc	+5Vd	I.L
D2202	74HCT00	14		7
D2203	74HCT4538	16		8
D2204	74HCT132	14		7
D2206	74HCT74	14		7
D2207	74HCT00	14		7
D2208	74HCT132	14		7
D2212	74HCT00	14		7
D2218	74HCT74	14		7
D2222	TEA1017		7	3

MAT 3263 II





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Figure 8.34.4 Unit A34 - TRIGGER CONTROL UNIT - circuit diagram.