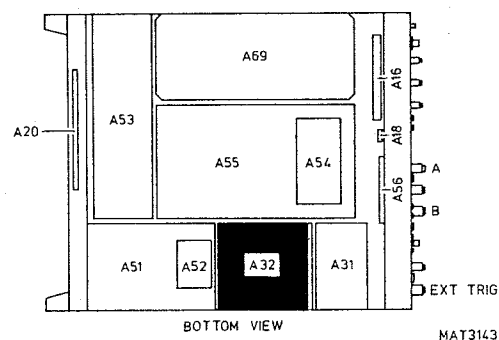


UNIT A32 - THREE STAGE TRIGGER UNIT

CONTENTS

8.32.1	General information.....	8.32-1
8.32.2	Three stage trigger circuit.....	8.32-1
8.32.3	Circuit description.....	8.32-4
8.32.4	Signal name list.....	8.32-6

8.32.1 General information

This unit consists of a trigger circuit that generates a trigger signal to start the fast ramp generator as the trigger signal crosses the trigger level with the correct slope and if the hold off time is elapsed. In the synchronised mode this signal is generated directly after the hold off time being elapsed. Furtheron, the units contains a filter amplifier for the trigger signal, followed by a number of divider stages. The output signals are applied to the trigger control circuit. The board is built up in SMD technology.

8.32.2 Three stage trigger circuit

The circuit consists of three schmitt trigger circuits (stages) in sequence (see figure 8.32.1).

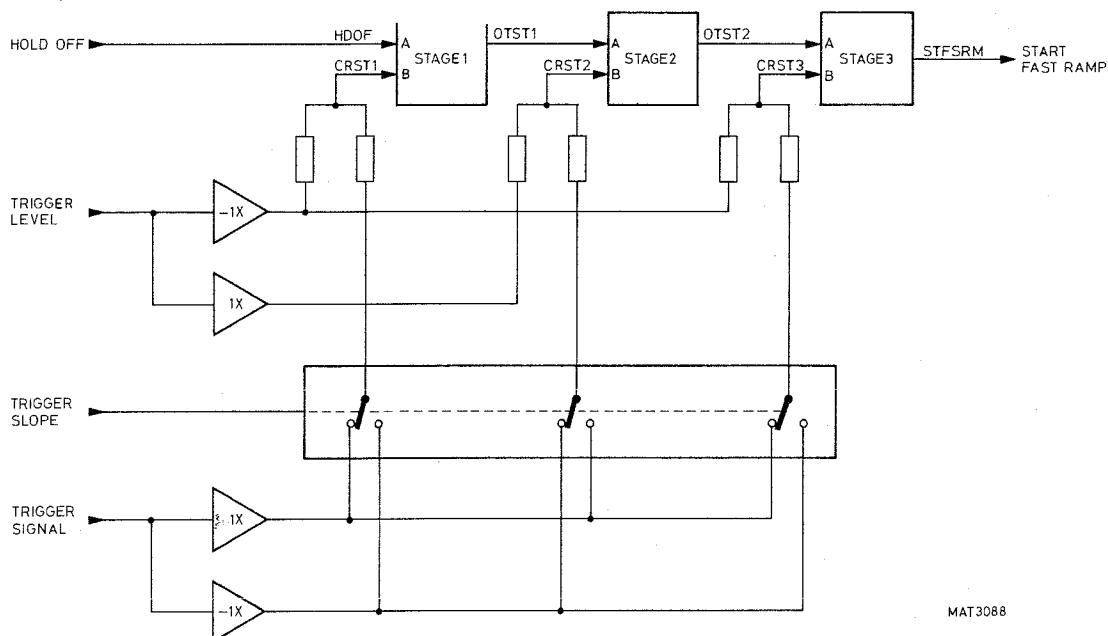
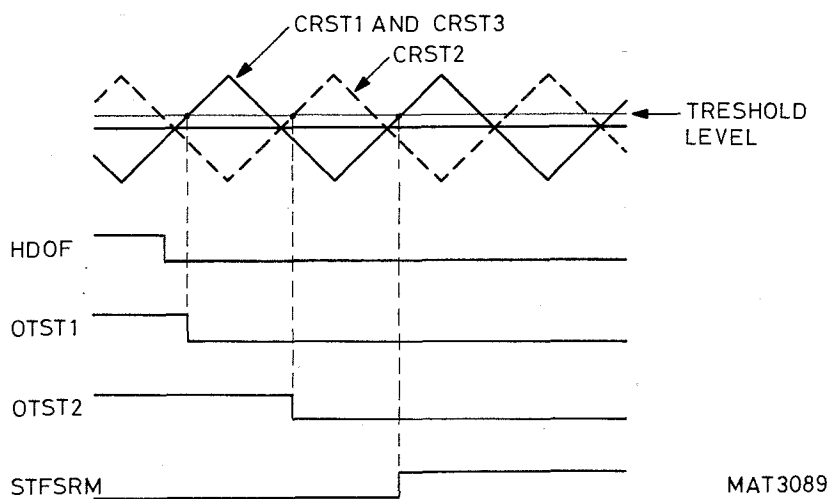


Figure 8.32.1 Block diagram of three stage trigger circuit.

Each stage has two inputs. Input B is non-inverting with a hysteresis. The output can only go high if input A is low. A conventional trigger circuit consists only of one of these stages. If the hold off time is elapsed, the A input (HDOF) is low. As soon as the trigger signal passes the trigger level, the output of the schmitt trigger goes high to start the fast ramp. Due to propagation delay times in the circuit, a small time uncertainty may arise if HDOF goes low at the moment that the trigger signal crosses the trigger level. This time jitter is unacceptable in this instrument. Therefore three stages are used.

Stage 1 and stage 3 get the trigger signal minus the trigger level, while stage 2 gets the trigger level minus the trigger signal.

The timing diagram in figure 8.32 shows how the three stages change over behind each other after the falling edge of HDOF, with the trigger level set at zero.



MAT3089

Figure 8.32.2 Timing diagram 1 of the three stage trigger circuit.

If HDOF goes low at the moment that CRST1 crosses the threshold level, or just a bit later, the signal OTST1 changes over immediately. Nevertheless OTST2 changes over almost a half period later. The same happens with STFSRM.

Figure 8.32.3 shows what happens if the trigger level is increased until triggering is just possible and HDOF goes low at the trigger moment. Now stage 1 changes over immediately at HDOF. If HDOF suffers from some jitter, the output of stage 1 will also jitter. Now stage 2 also suffers from some jitter, because it changes over just behind stage 1.

Nevertheless stage 3 changes over almost one period later, so this stage will not suffer from jitter and the fast ramp starts at a fixed moment.

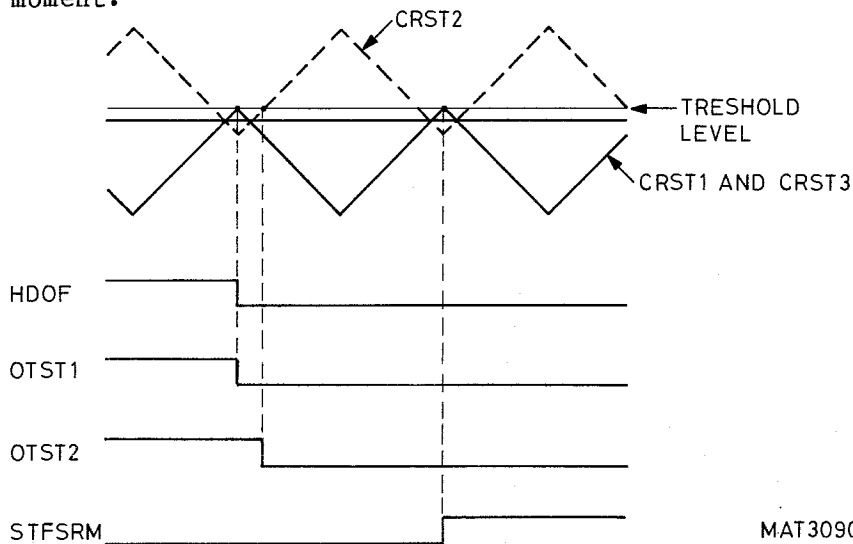


Figure 8.32.3 Timing diagram 2 of the three stage trigger circuit.

In synchronised mode all three stages should change over immediately behind each other when HDOF goes low.

This realised by some auxiliar circuits, which are not indicated in figure 8.32.1.

These circuits pull the B-inputs down. So after the falling edge of HDOF, all three stages change over immediately behind each other.

The edges of the HDOF signal are less steep in synchronised mode (see also section 8.51.3). On these slow rising/falling edges, the trigger signal is superimposed by another auxiliar circuit.

The change over of the three stages is now influenced by the trigger signal. This results is a synchronized mode with a lock range.

A signal which is displayed stable, remains stable in spite of minor changes in the hold off time, e.g. due to drift.

8.32.3 Circuit description

The circuits described in section 8.32.2 are realised with current controlled circuits.

As the three stage of the three stage trigger circuit are almost identical only STAGE 1 will be described.

The hart of the stage is a flip-flop circuit, consisting of transistors V5206, V5207, V5203 and V5204.

Furtheron there is an output buffer (V5212 and V5213) and a buffer in a positive feedback circuit (V5209 and V5211).

During the hold off time the status of the transistors is as given in the table below:

Conducts	Blocks
V5201	V5208
V5207	V5206
V5203	V5204
V5213	V5212
V5202	
V5211	V5209

After the hold off time, transistor V5201 blocks. The current which is sunk to CRST1 via diode V5257 depends on the trigger level and the trigger signal.

When the trigger signal passes the trigger level, transistor V5202 will block and all transistors will change over.

The positive feedback line via transistor V5211 speeds up the changing over and creates some hysteresis.

In SYNCHRONIZED MODE, signal SYSG is derived from the trigger signal and is coupled to the base of transistor V5208 via capacitor C5201. In this way it is added to the hold off signal HDOF to obtain a lock range. In the triggered mode there is a fixed DC level applied to capacitor C5201.

The LEVEL CONTROL circuit sinks a current, depending on the selected trigger level from the 3 control points of the stages (CRST1, CRST2 and CRST3). If the trigger level is increased, the current through X5207 (TRLV-1) to resistor R5298 increases. Therefore the voltage at measuring point X30 rises. The current which is sunk from CRST2 will increase and the currents from CRST1 and CRST3 will decrease. Note that the voltage at measuring point X29 remains constant.

The SYNC CONTROL B circuit sinks a current from CRST2 in SYNCHRONIZED MODE, because SYM0--LT is low.

Now STAGE 2 changes over immediately when OTST1 goes low.

Stage 3 has a different output stage, to control the FAST RAMP GENERATOR on the FAST RAMP UNIT A52.

The trigger signal (TRSG) from the TRIGGER INPUT unit A31 is buffered, amplified and split into symmetrical signals TRSG1 and TRSG2 by the BUFFER circuit around IC D5206. These two signals sink currents in the SLOPE CONTROL circuit from CRST1, CRST2 and CRST3 depending on the TRSP signal, according to the following table.

	TRSP	TRSG1	TRSG2
POS SLOPE	LOW	CRST2	CRST1+CRST2
NEG SLOPE	HIGH	CRST1+CRST2	CRST2

Furtheron the SLOPE CONTROL circuit has a potentiometer to adjust the trigger gap (R5397).

In synchronized mode, the SYNC CONTROL A circuit unbalances the BUFFER and the SLOPE CONTROL in such a way that STAGE 1 and STAGE 3 change over immediately after the falling edge of HDOF. As already mentioned the SYNC CONTROL B circuit takes care that STAGE 2 changes over immediately.

The FILTER/AMPLIFIER amplifies and filters the trigger signal from the TRIGGER INPUT unit A31 and splits it into two symmetrical signals TRSGFL-1 and TRSGFL-2, which are applied to dividers.

The higher order filter cuts off frequencies above 175 MHz, which cannot be processed by the following hardware.

The DIVIDER HIGH AMPL consists of a schmitt trigger circuit (D5494, R5461 and R5462), followed by 4 divide-by-four stages.

The schmitt trigger gives an output signal if the input signal of the oscilloscope is 20 mVp-p or more (in SENS HIGH mode).

The DIVIDER LOW AMPL is similar to the DIVIDER HIGH AMPL. The schmitt trigger (D5494, R5458 and R5459) gives an output signal if the input signal of the oscilloscope is 10 mVp-p or more (in SENS HIGH mode).

The signal at pin 11 of IC D5498 is divided by two by another divider stage.

The dividers are built up with ECL circuits.

The three output buffers (D5499) convert the signals to TTL level, resulting in TRSGHA, TRSGLA and TRSGLA-2, which are routed to the TRIGGER CONTROL UNIT A34.

In synchronized mode, the SYNC CONTROL C amplifies the filtered trigger signal from the transistor in D5204 (pin 2) and applies it as signal SYSG to STAGE 1, where it is added to the hold off signal, to obtain a lock range for the synchronized mode. In triggered mode SYSG is at fixed DC level.

Note: This unit forms together with the Time-base unit A51 and the Fast Ramp unit A52 a closed loop (see also figure 8.51.1). When a unit hangs up the loop can be opened by disconnecting the coax cable at X5202 (HDOF).

By applying a square wave of 1 kHz with an amplitude of 400 mVp-p symmetrically around zero to X5202 the correct operation of these units can be checked, if an input signal is present to generate triggers.

8.32.4 Signal name list

UNIT 32

Signal name	Description	Signal source	Signal destination(s)
CRST1	Control stage 1	A32	A32
CRST2	Control stage 2	A32	A32
CRST3	Control stage 3	A32	A32
HDOF	Hold off	A52	-
OTST1	Output stage 1	A32	A32
OTST2	Output stage 2	A32	A32
STFSRMHX	Start fast ramp	A32	A52
STFSRMLX	Start fast ramp	A32	A52
SYMO--LT	Synchronized mode	A34	-
SYSG	Synchronize signal	A32	A32
TRVL-1	Trigger level 1	A34	-
TRSG	Trigger signal	A31	-
TRSG1	Trigger signal 1	A32	A32
TRSG2	Trigger signal 2	A32	A32
TRSGFL-1	Trigger signal filtered 1	A32	A32
TRSGFL-2	Trigger signal filtered 2	A32	A32
TRSGHA	Trigger signal high amplitude	A32	A34
TRSGLA	Trigger signal low amplitude	A32	A34
TRSGLA-2	Trigger signal low amplitude 2	A32	A34
TRSP	Trigger slope	A34	-

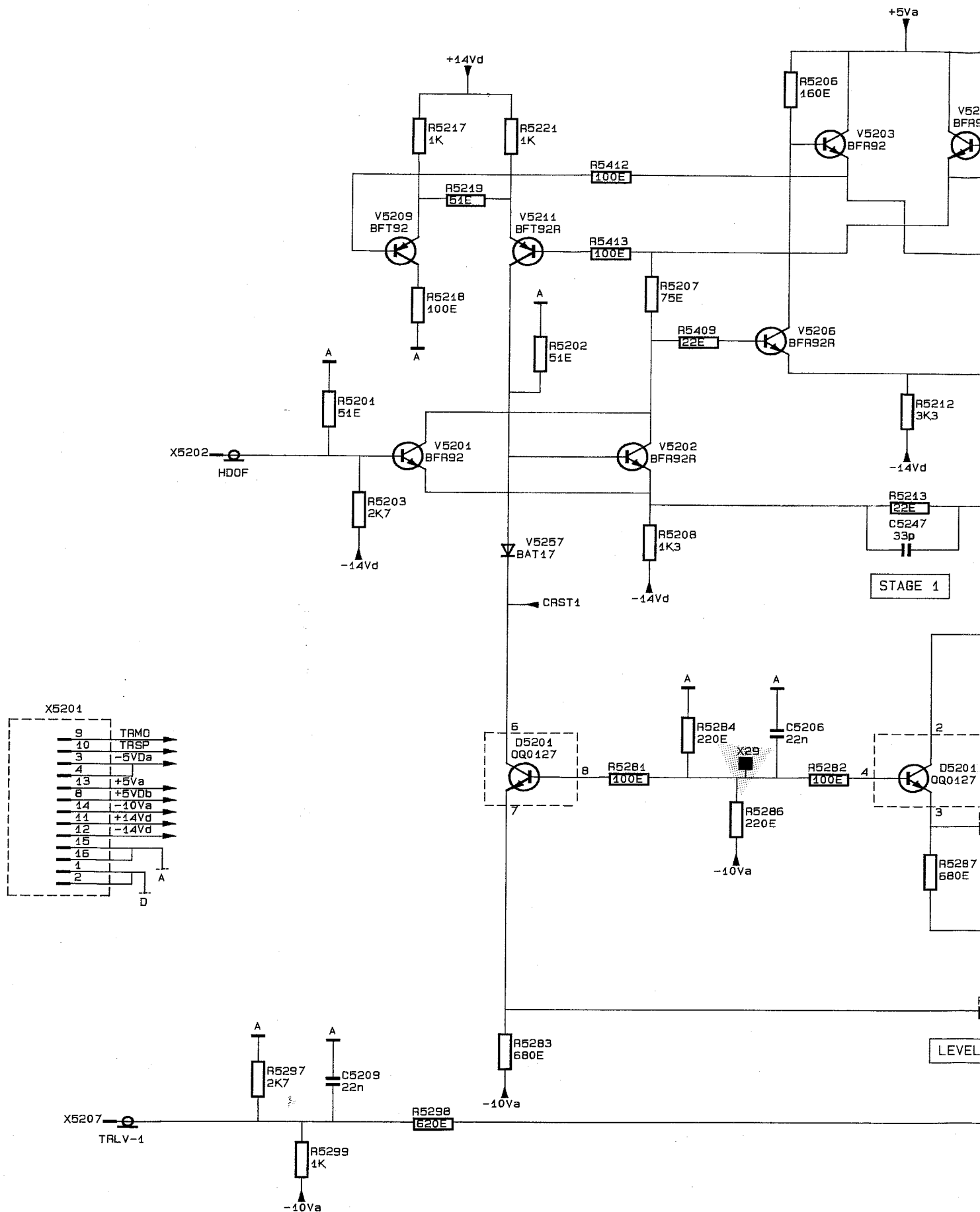
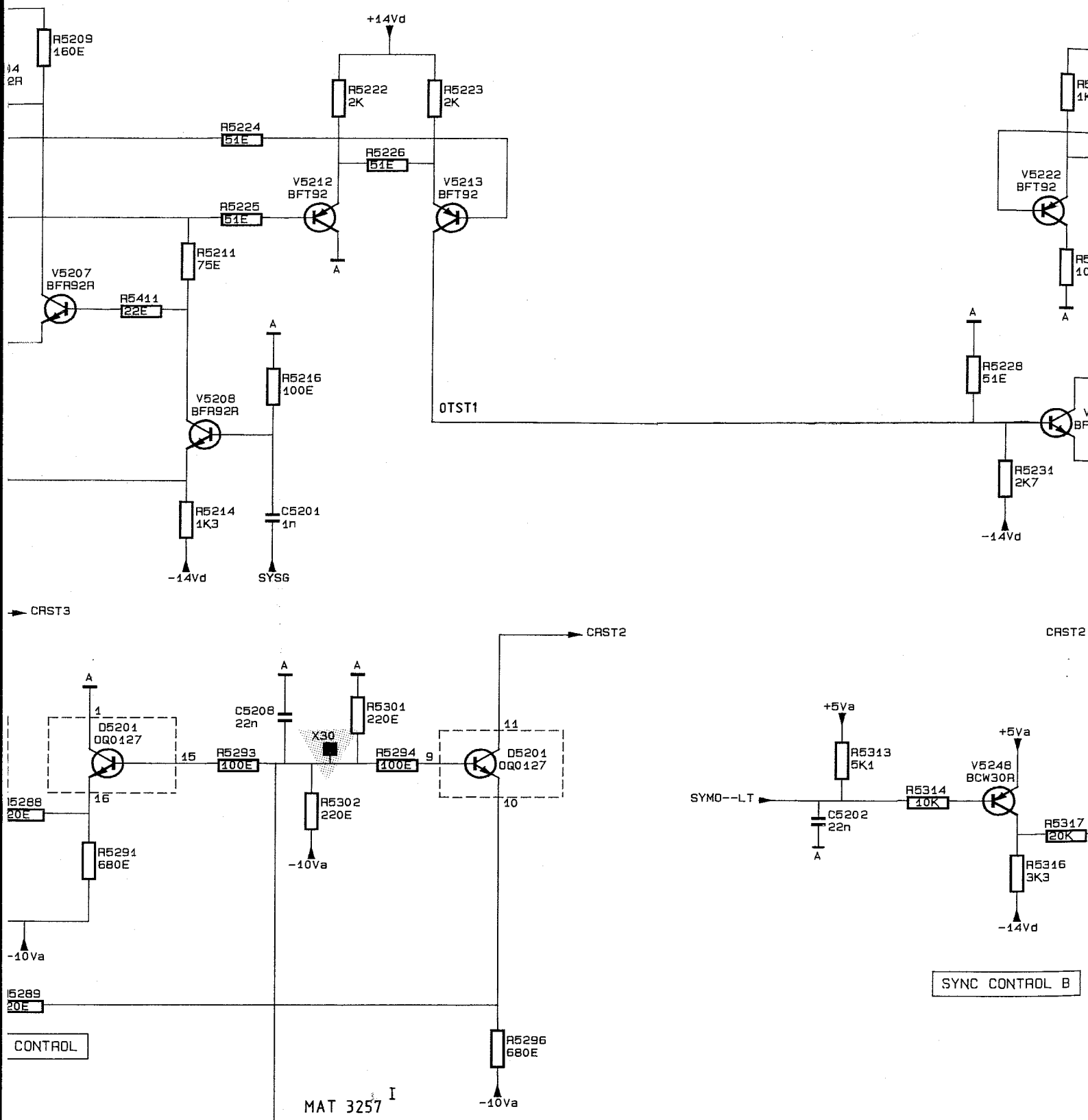
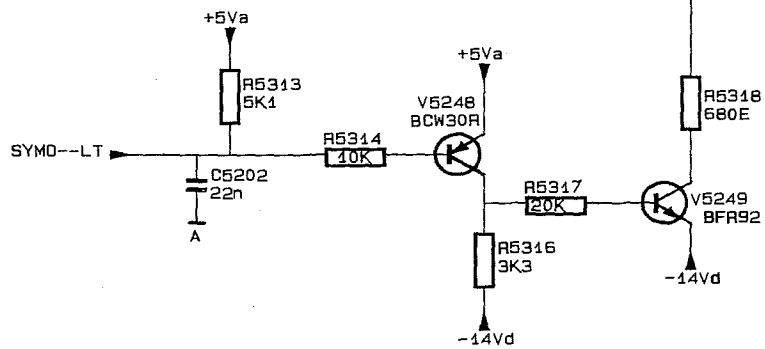
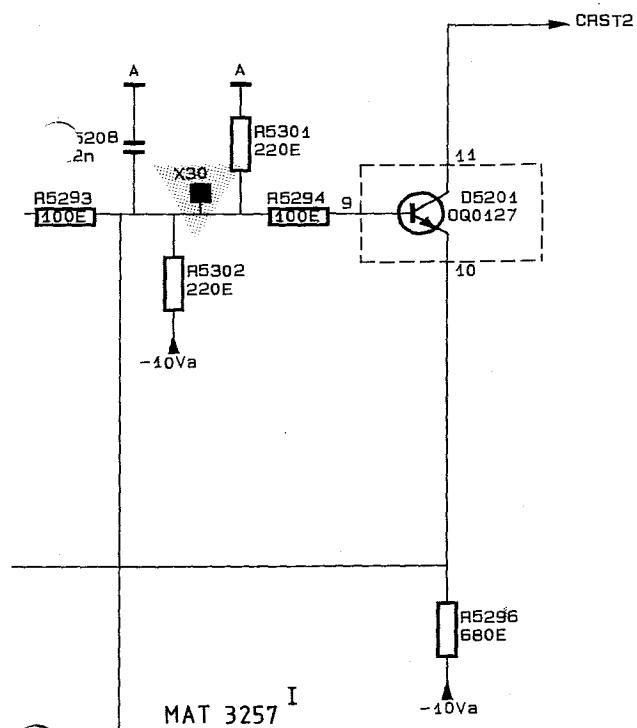
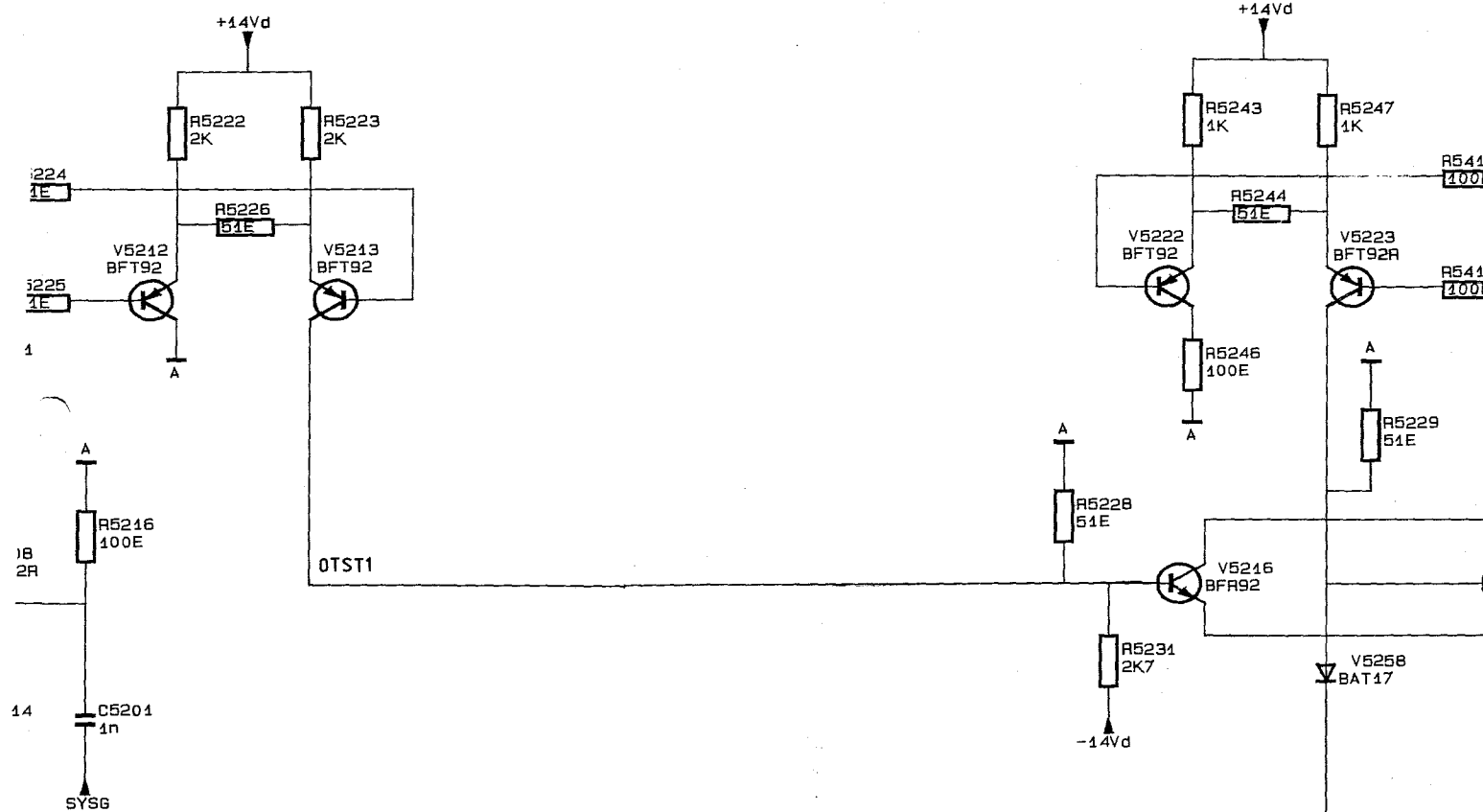
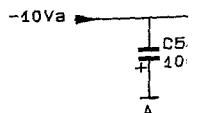
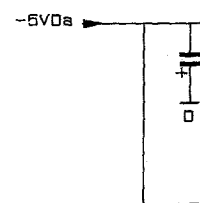
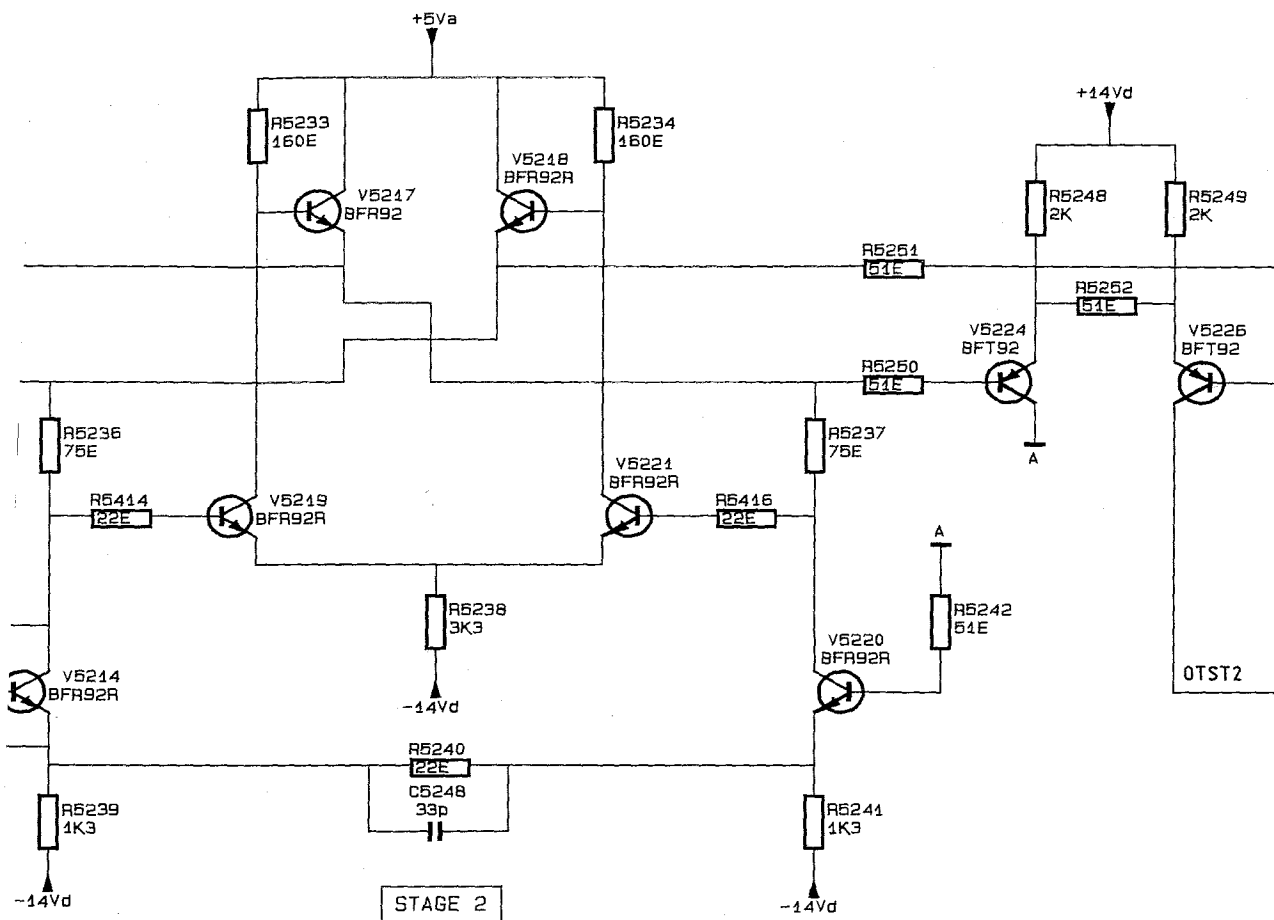


Figure 8.32.5 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.

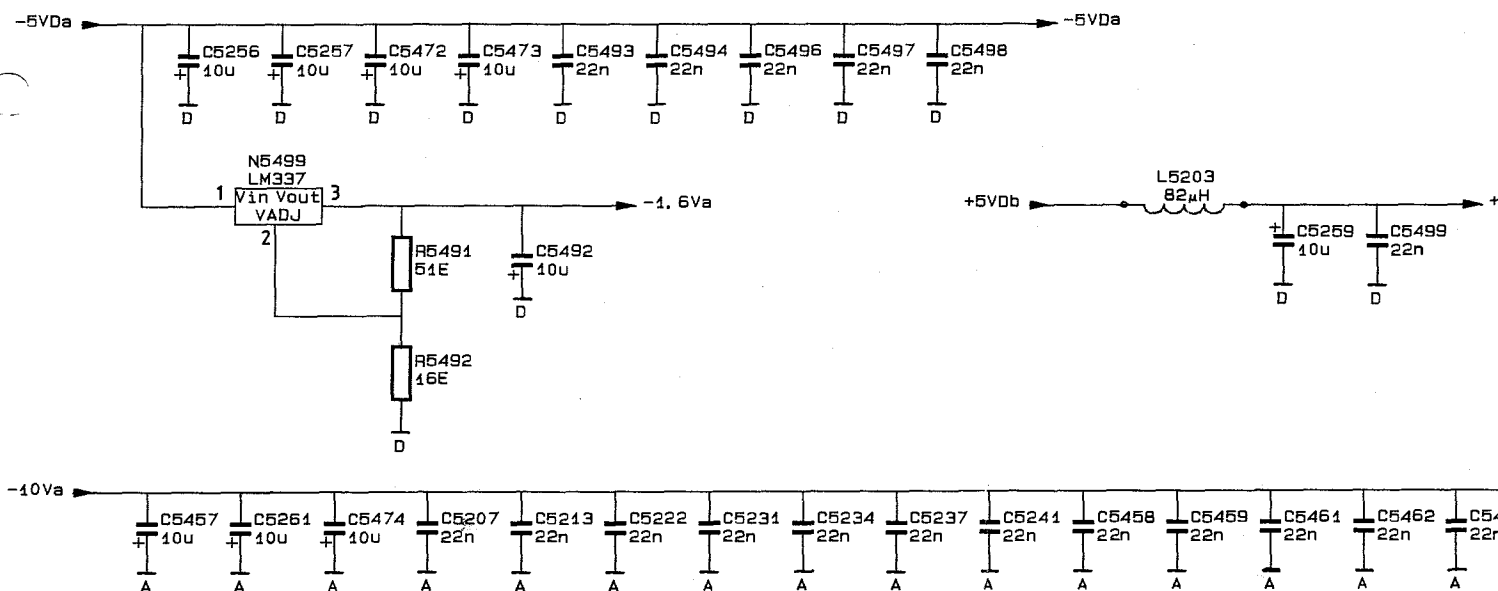
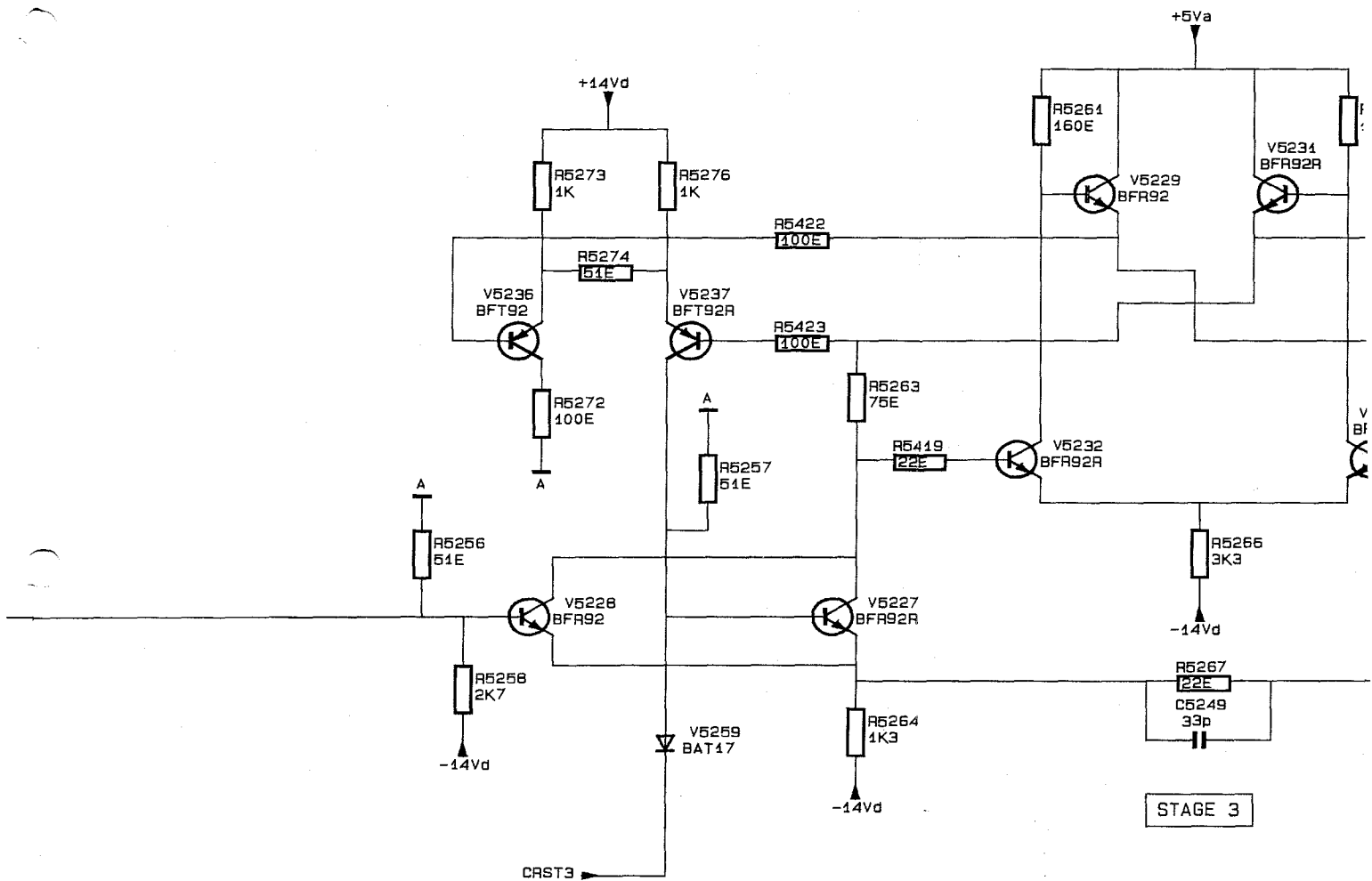


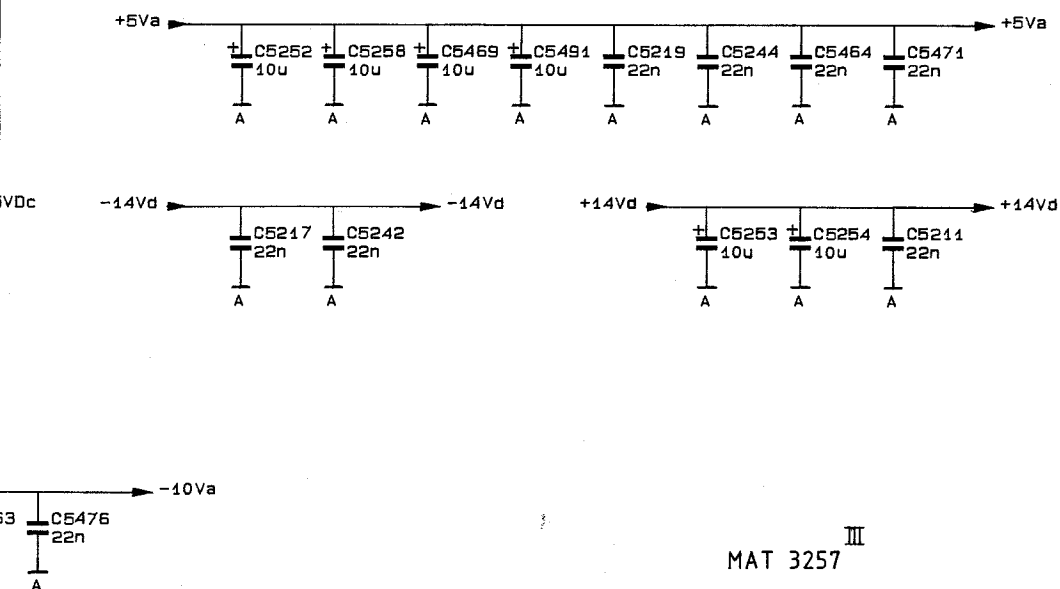
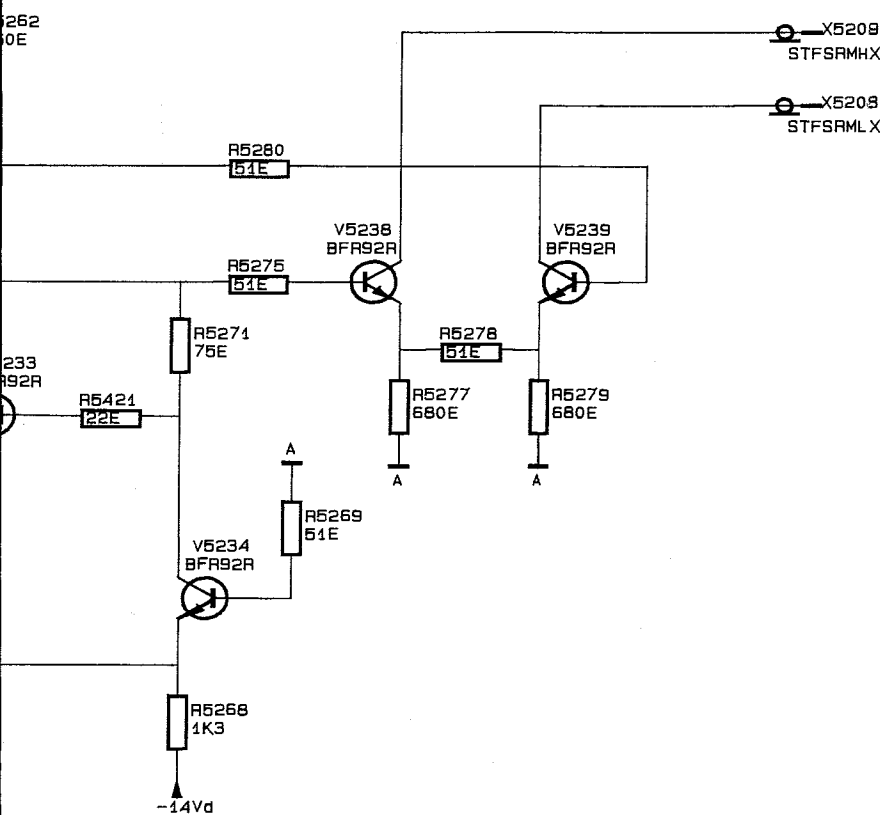


SYNC CONTROL B



MAT 3257 II





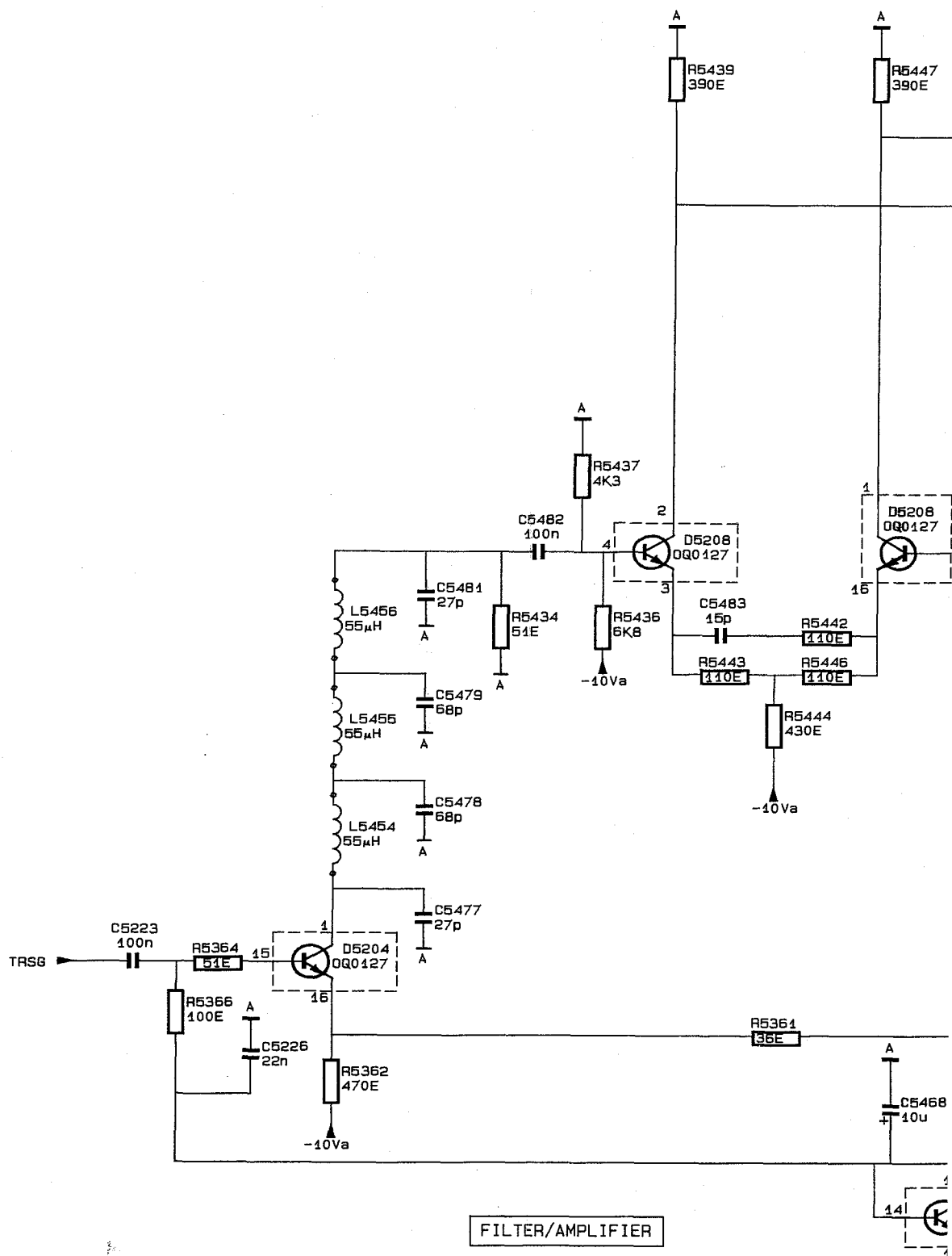
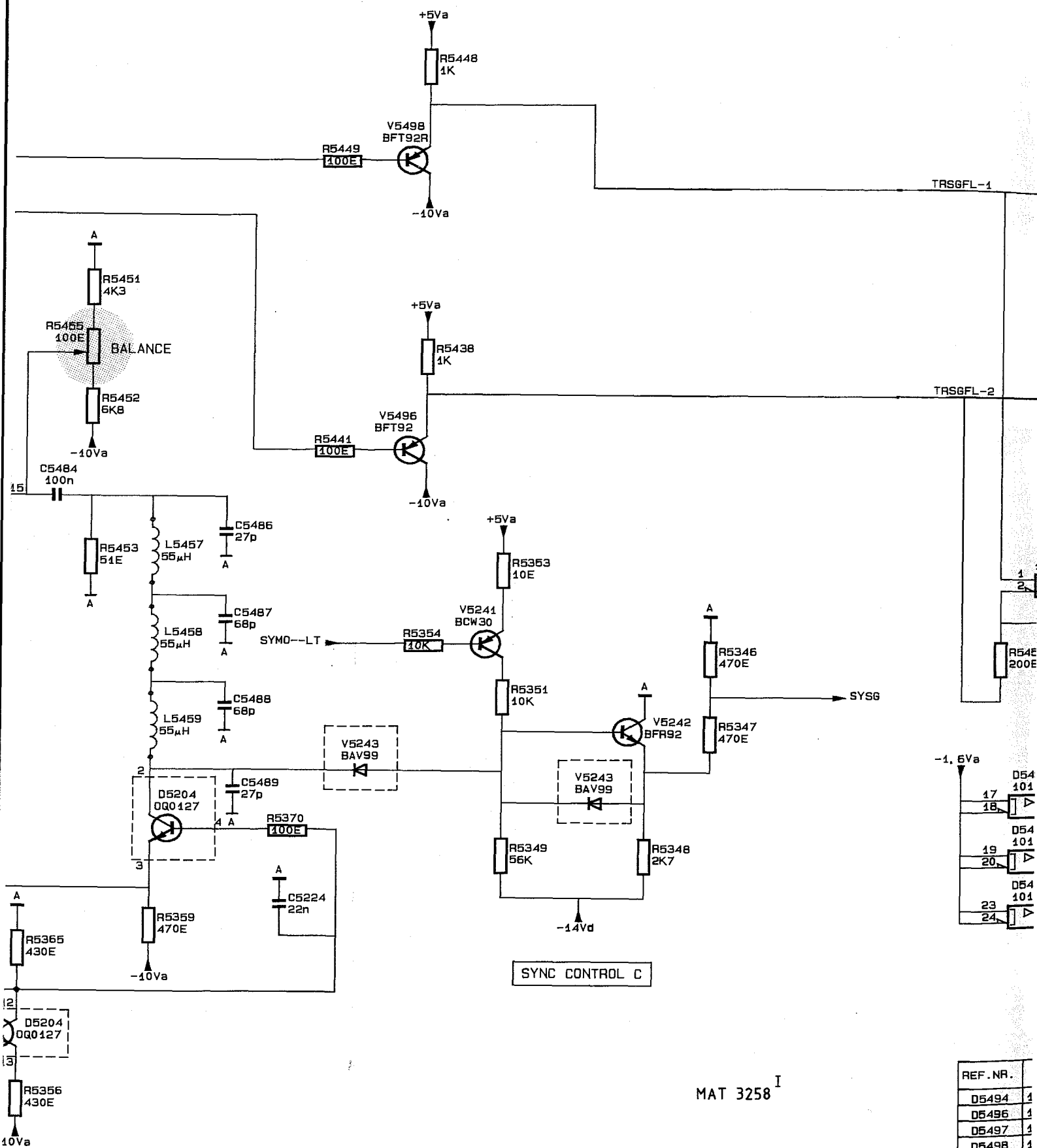
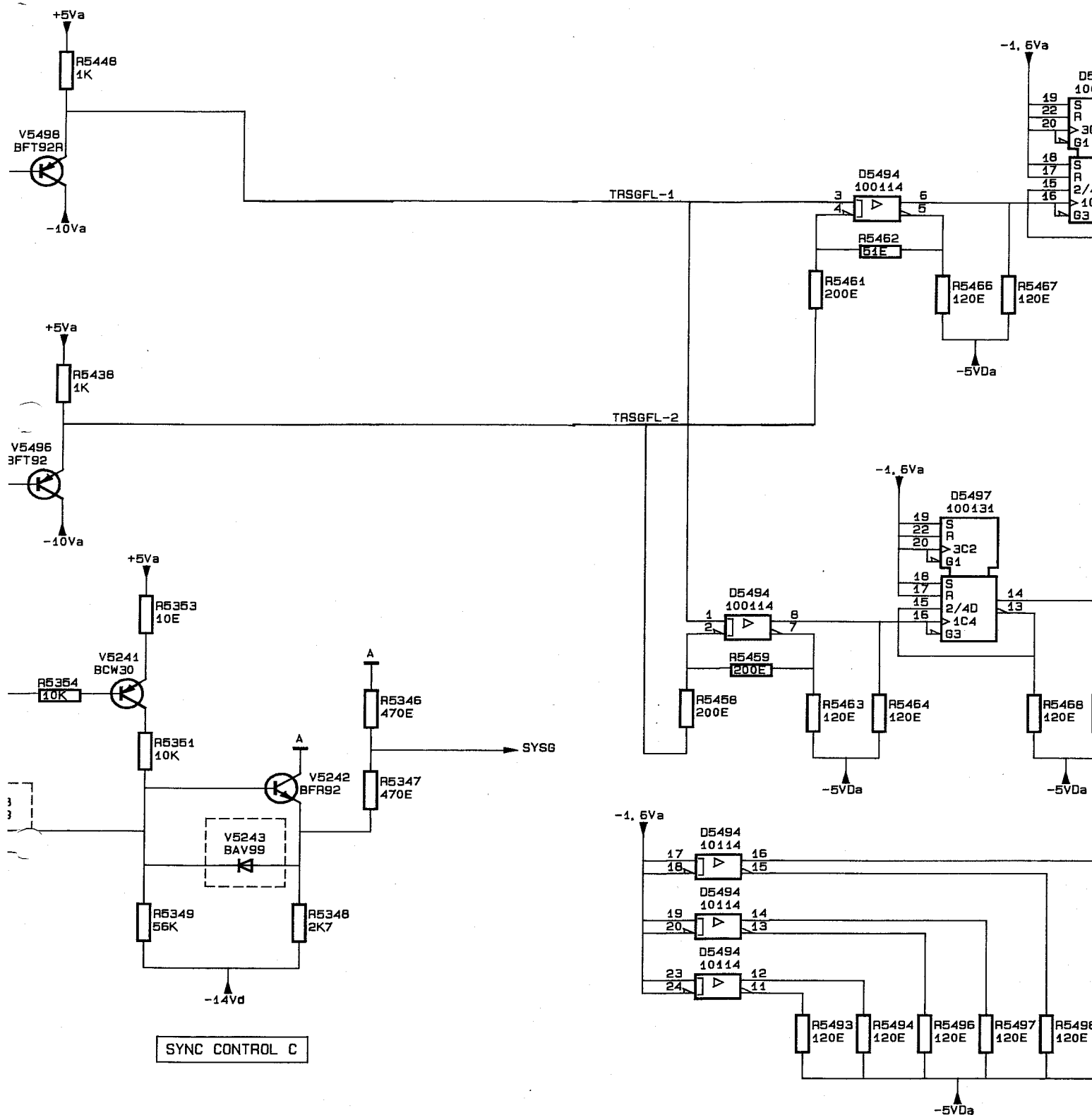


Figure 8.32.6 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.



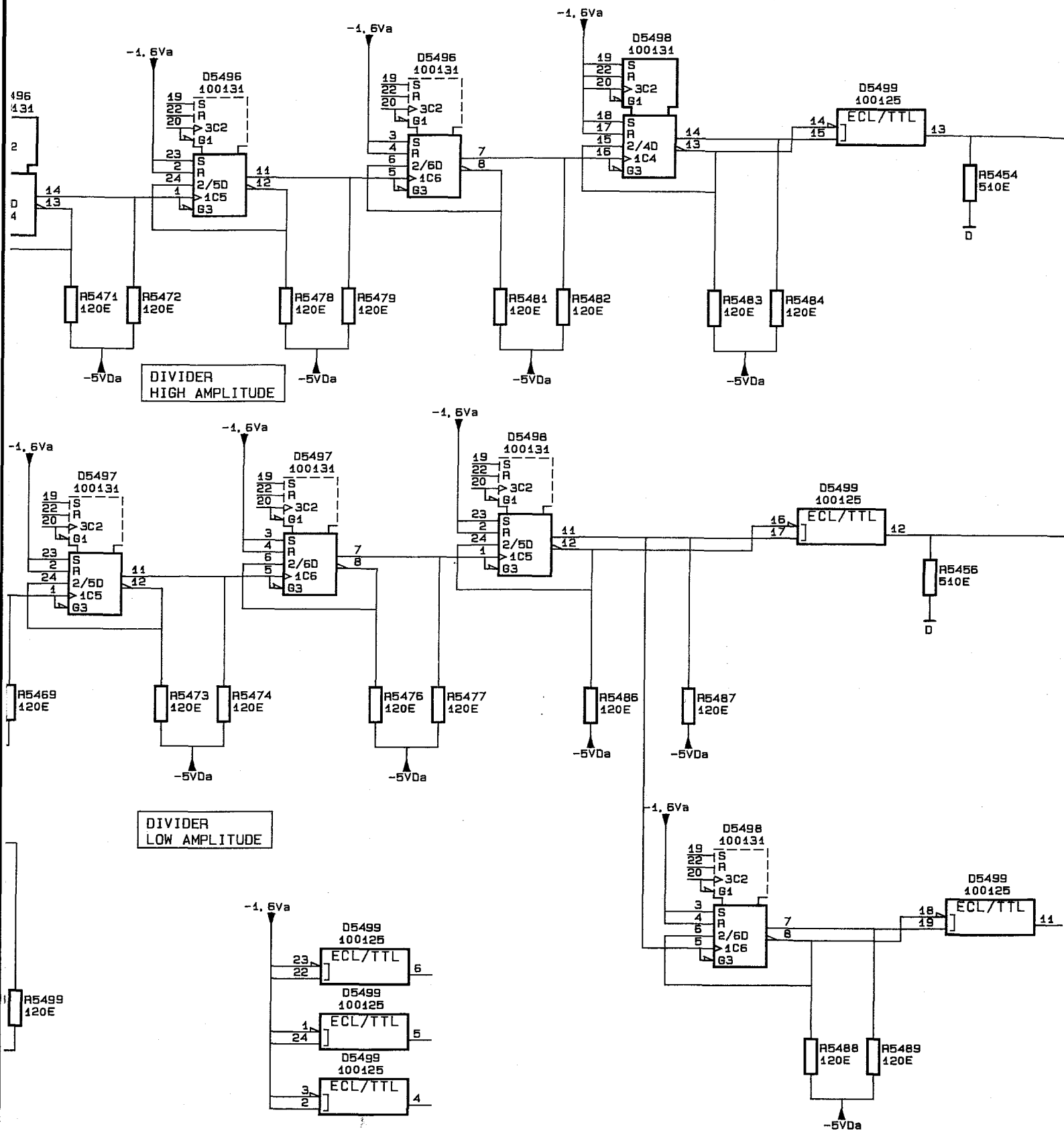
MAT 3258 I

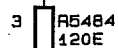
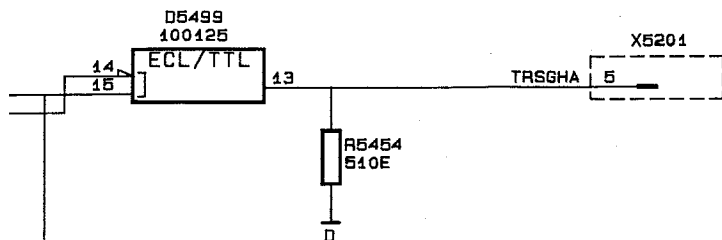
REF. NR.	
D5494	1
D5496	1
D5497	1
D5498	1
D5499	1



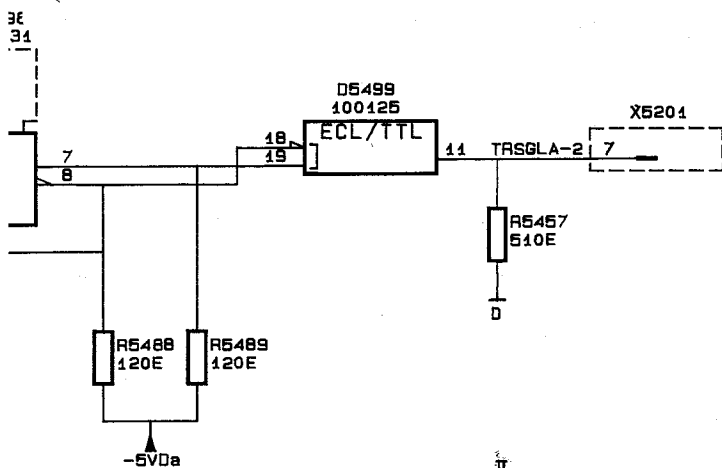
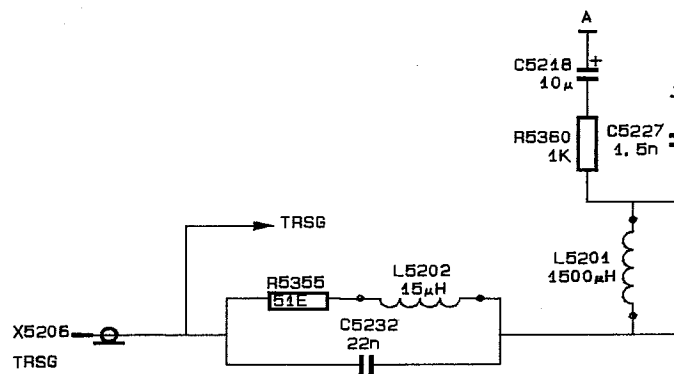
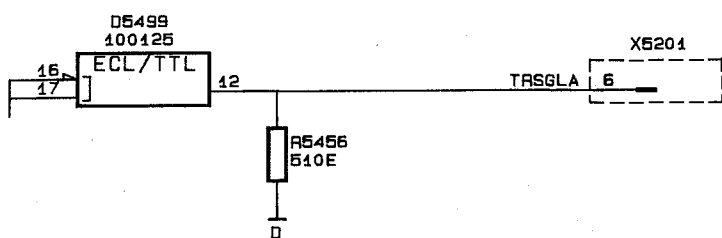
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REF. NR.	TYPE	-5Vd	+5Vd	D
D5494	100114	21		9-10
D5496	100131	21		9-10
D5497	100131	21		9-10
D5498	100131	21		9-10
D5499	100125	21	7-8	9-10

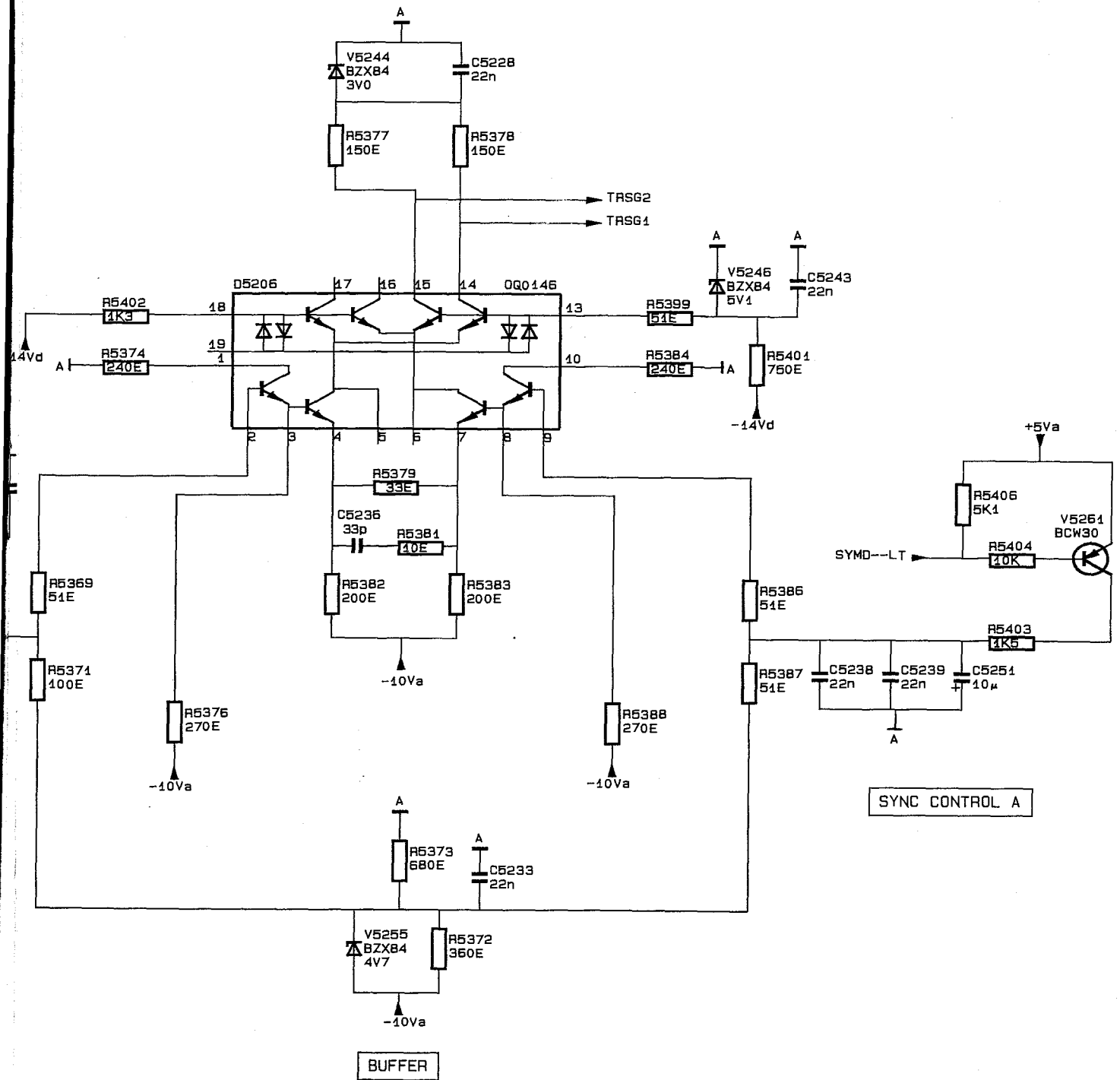




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MAT 3258 II



MAT 3259

Figure 8.32.7 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.

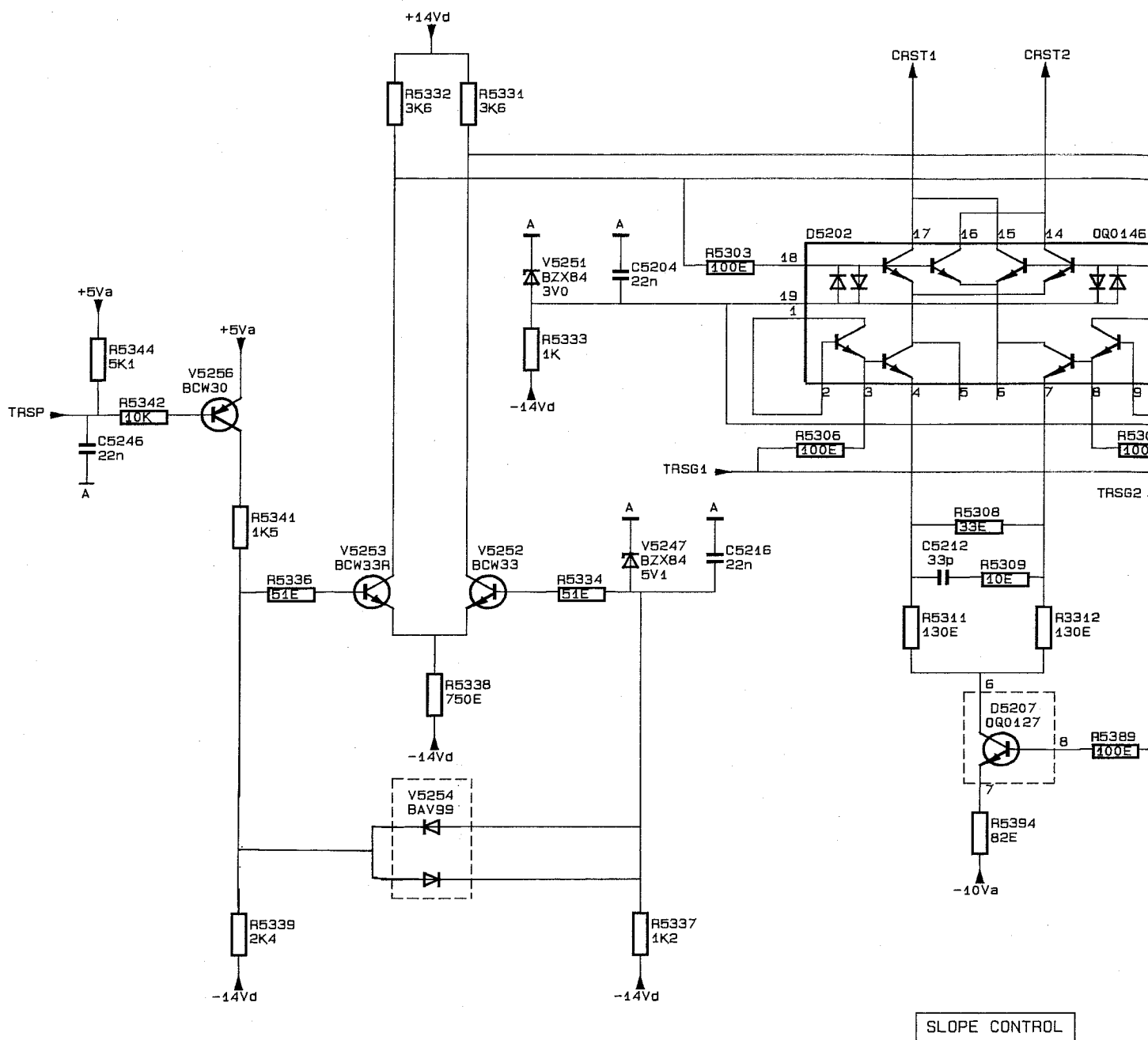
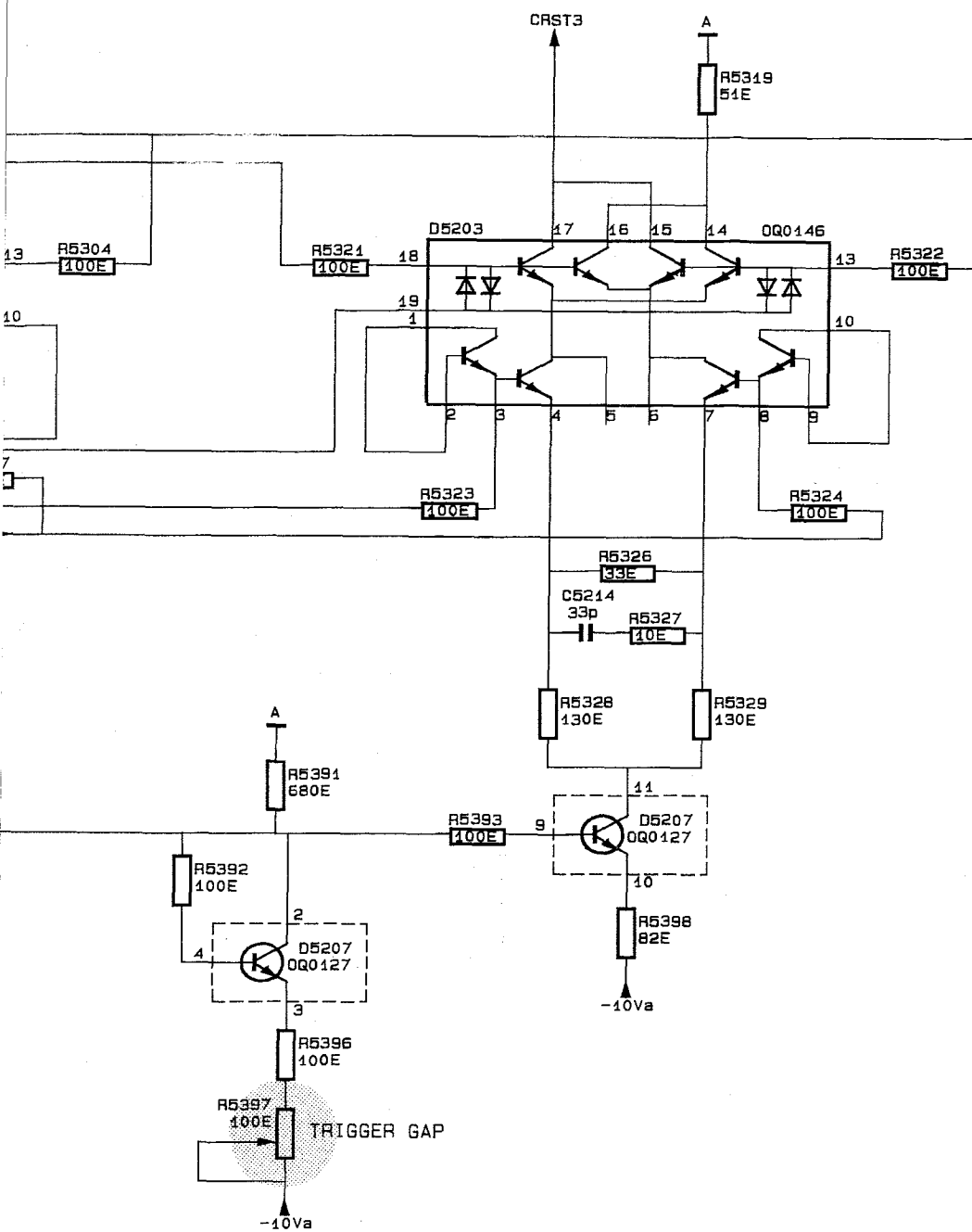


Figure 8.32.8 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.



MAT 3260