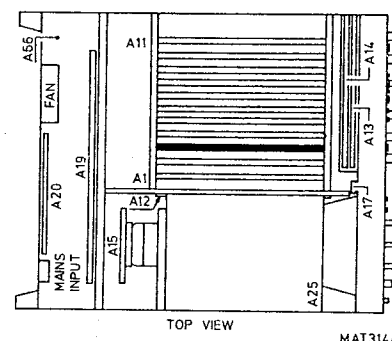


UNIT A3 - DISPLAY CONTROL UNITCONTENTS

8.3.1	General information.....	8.3-1
8.3.2	Display system and timing.....	8.3-2
8.3.3	Circuit descriptions.....	8.3-7
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8.3.1 General information

This unit contains the circuits needed to control the display circuits on units A2 and A4.

It contains the following circuits:

Data buffer

Preset register

Output ports for display parameters

Display address counter

Data buffers for:

- Display address data
- Softkey text data
- Line text data

Timing circuits:

- Synchronization flip flops
- Data acknowledge flip flop
- Start flip flop
- Smooth delay flip flop

Z + interrupt timer

Z - counter

Interrupt counter + interrupt flip flop

Restart counter

Address decoder

Z - detection circuit

Clock-phase generator

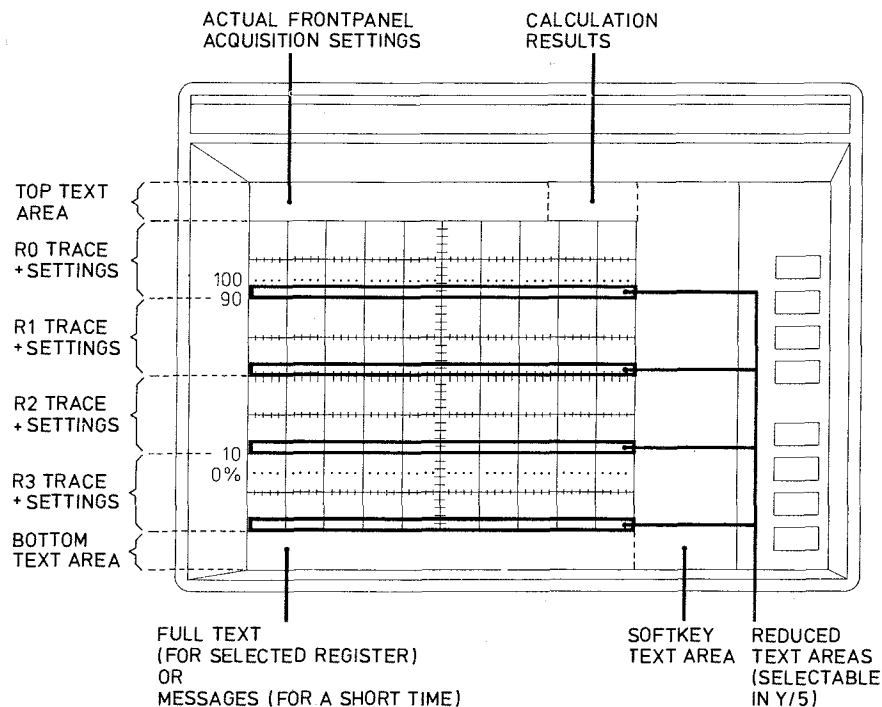
Memory select circuit

8.3-2

8.3.2 Display system and timing

8.3.2.1 Screen lay out

The screen lay out is as follows.



MAT2422
861017

Figure 8.3.1 Screen lay out.

8.3.2.2 Display cycle

During each complete display cycle of about 19 ms the complete contents of the trace memory as well as the text memory is displayed on the C.R.T. screen.

Each display cycle consists of the following display blocks in sequence:

R0 A and/or R0 B	}	
R1 A and/or R1 B	}	Contents of the
R2 A and/or R2 B	}	trace memory
R3 A and/or R3 B	}	
TAT		Top text area
RAT R0		Reduced area text R0
RAT R1		Reduced area text R1
RAT R2		Reduced area text R2
RAT R3		Reduced area text R3
BAT		Bottom text area
SKT		Softkey area text
MSC	}	Miscellaneous text (like cursors and channel identification)
PLOT		One dot to plot

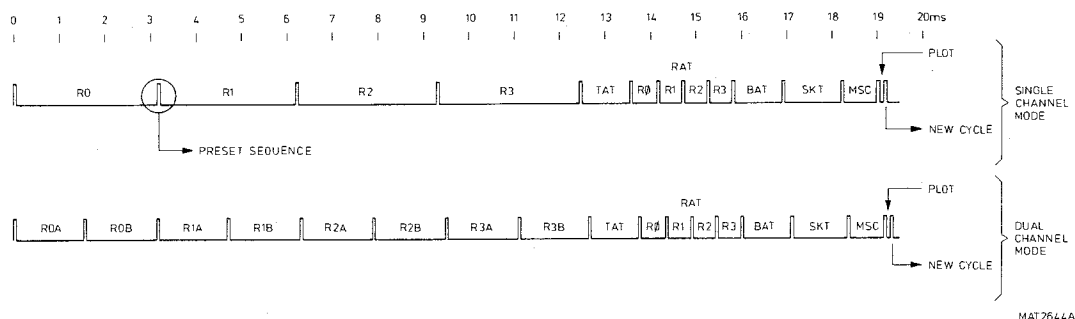


Figure 8.3.2 Display cycle.

8.3.2.3 Preset sequence

After the display of each display block an interrupt level signal IL05--LT is send to the microprocessor. The processor in turn starts a preset sequence of new preset values and new parameters for the display circuits. At the end of this preset sequence, signal WRDPSTLT is generated and the display of the next display cycle is started.

Presetting is done in the following sequence:

- 1 Read overflow bit from DB00
- 2 WRVEPOLT Write the vertical position data to the VERTICAL POSITION LATCH D2314 and D2316 on unit A2.
- 3 WRHOPOLT Write the horizontal position data to the HORIZONTAL POSITION LATCH D2317 and D2318 on unit A2.
- 4 WRPSDPLT Write the preset data for the display address counter to the PRESET REGISTER D2103 and D2104 on unit A3.

This is done together with the setting of the signals for the PLOT interface:

PLOT	0 = No sample in S&H
	1 = Sample in S&H
PU----LT	0 = Pen-up
	1 = Pen-down
PFPY	0 = Pen-up (high)
	1 = Pen-up (low)
PLZEOT	0 = Plot output active
	1 = Plot output not active

These four signals are only generated when a plot action has to be performed.

5 WRDPPALT

Write the display parameters which are listed below, to the OUTPUT PORTS DISPLAY PARAMETERS D2106 and D2107 on unit A3.

DPMY02	DPMY01	DPMY00	DISPLAY BLOCK
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	Text TAT/RAT
1	0	1	Text BAT/SKT/MSK
1	1	0	--
1	1	1	--

DPMO--LT Display mode

0 = Dual channel

1 = Single channel

CHID Channel identity

0 = Channel A

1 = Channel B

HOMO Horizontal mode

0 = X=t

1 = AvsB (or text)

SM----LT Smooth

0 = Smooth

1 = No smooth

DIDJ Disable dot join

0 = No dots, dot joined

1 = Dots (or text)

IVDCDB Invert display control databus

0 = No invert

1 = Invert

SVR1 Save to R1

0 = No save

1 = Save

SVR2--LT Save to R2

0 = No save

1 = Save

SVR3 Save to R3

0 = No save

1 = Save

SAVE--LT Save

0 = Save

1 = No save

ENTXLNLT Enable text lines

0 = TAT, RAT, BAT

1 = Other text

ENTXSKLT Enable text softkey

0 = SKT

1 = Other text

Z-AC Z-active

0 = No light

1 = Light

6 WRHOVRLT Write data to the OUTPUT PORT DISPLAY PARAMETERS
D2108 on unit A3 and to the X VARIABLE LATCH D2332
on unit A2.

This is done together with the following signals:

EPY-01	EPY-00	Y-EXPAND
0	0	* 1/4 - Trace
0	1	* 1 - Trace + MSC text
1	0	* 4 - Text (Other)
1	1	* 4 - Trace

EPX-02	EPX-01	EPX-00	X-EXPAND
0	0	0	*1
0	0	1	*2
0	1	0	*4
0	1	1	*8
1	0	0	--
1	0	1	*16
1	1	0	*32
1	1	1	*64

TXLNSKLT Text line + softkey
0 = TAT, RAT, BAT, SKT
1 = Trace + MSC
DIOS--HT Disable overscan
0 = Overscan
1 = No overscan

7 Initialization of Z-counter 0

8 Initialization of Z-counter 1

9 Initialization of Z-counter 2

10 Preset of LSB countvalue of Z-counter 0

11 Preset of MSB countvalue of Z-counter 0

12 Preset of LSB countvalue of Z-counter 2

13 Preset of MSB countvalue of Z-counter 2

14 Preset of LSB countvalue of Z-counter 3

15 Preset of MSB countvalue of Z-counter 3

16 Clear instruction (read)

17 WRDPSTLT Start display of the next display block after the
setting of the parameters

8.3.2.4 Display timing

The display timing is arranged in such a way that one dot is displayed per 750 ns. Each period of 750 ns is divided into three fases of 250 ns each like shown in the following figure.

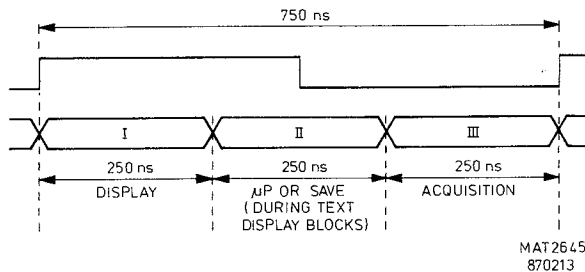


Figure 8.3.3 Display timing.

Fase I is for display actions, fase II for UP or SAVE actions and during fase III acquisition actions can be performed.

8.3.2.5 SAVE timing

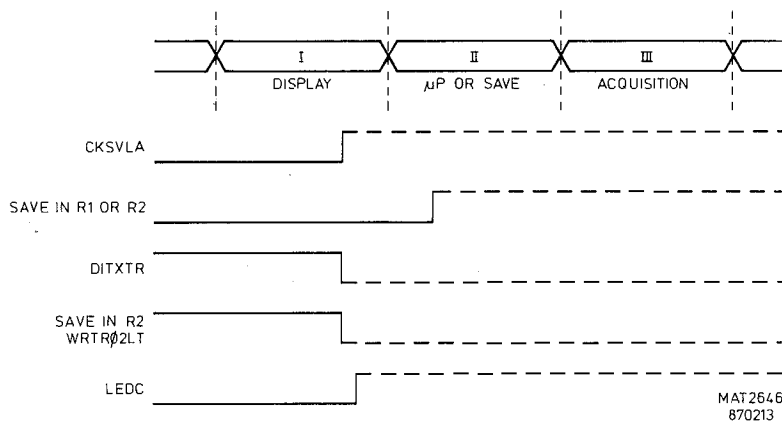


Figure 8.3.4 Save timing.

A save action from R0 to R1, R2 or R3 is done during the display of text blocks. It is done with the first 4096 addresses of the total of 8192 addresses which are generated by the display address counter. Each address is applied to register R0, to the selected register and to the text memory.

The output data of R0 is latched in the SAVE latch during FASE I with signal CLKVLA.

If R2 is selected for a save action, this register is enabled directly to store the data value.

When this is done, the output of R0 is disabled and the output of the text memory is placed on the trace data bus via the TEXT/TRACE buffer via signal DITXTR. The text can be displayed then.

If R1 or R3 is selected, the output of the SAVE latch is placed on the trace data bus during FASE III, address line TRAB13 is switched to "1" to point to R1 or R3 and the relevant chip select signal is activated.

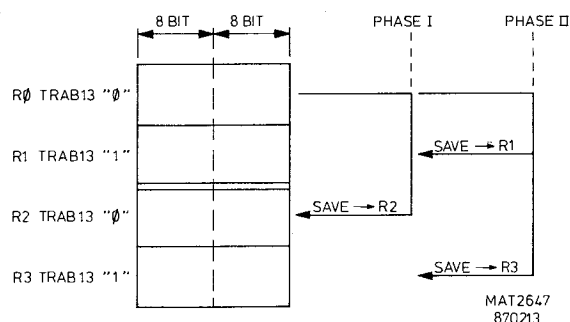


Figure 8.3.5 Save actions.

8.3.3 Circuit descriptions

8.3.2.1 Data buffer

Data from the microprocessor system on the data lines DB00...15, which is meant for the DISPLAY CONTROL unit A3, is applied to the internal display data bus lines DPDB00...15 of this unit. This data is transferred via the DATA BUFFER, which consists of D2101 and D2102 when the I/O select signal IOSL05LT is activated.

8.3.3.2 Preset register

Preset data from the microprocessor system can be latched in the PRESET REGISTER D2103 and D2104 (partly) when the write pulse WRPSDPLT is generated at the beginning of each new display block. The data on the data lines PSDP00... PSDP11 is used to preset the DISPLAY ADDRESS COUNTER with a start value for the next display action. This value depends on the channel which is selected for display, the selected horizontal expand factor or the value which has to be plotted.

8.3.3.3 Output ports display parameters

A number of display parameters can be latched in the OUTPUT PORTS DISPLAY PARAMETERS D2104 (partly), D2106, D2107 and D2108 as described under section 8.3.2.

8.3.3.4 Display address counter

The DISPLAY ADDRESS COUNTER, consisting of the counters D2111, D2112 and D2113, generates the addresses of the TRACE MEMORY locations to be displayed.

The counter is normally (in single channel mode) presetted to its zero state before a display block starts and the counter counts through its complete range during a display block.

In dual channel mode however, the counter needs to know whether channel A or channel B has to be displayed. The correct start address of the channel in the TRACE MEMORY has to be presetted by the microprocessor system. The counter counts then with a speed which is twice the speed in single channel mode.

The counter is always presetted by the value which is present in the PRESET REGISTER at the beginning of a display block. Presetting is done under the control of signal DIDPPS. Presetting is stopped at the start of a display block with signal STDP via flip flop D2114. Counting is started then under the control of signal DIDPCN.

The first output bit DPAB00 of the display counter is via multiplexer D2118 applied to the display address bus and influenced depending on the selection of single or dual channel mode.

Single channel mode: (HOMO = "0" and DPMO--LT = "1")

DPAB00 = DPAB00

Dual channel mode: (HOMO = "0" and DPMO--LT = "0")

DPAB00 = CHID (Channel identification)

CHID = "0" means channel B (odd locations in memory)

CHID = "1" means channel A (even locations in memory)

In dual channel mode, the display counter clockpulse DPCNCK is switched to a speed which is twice the speed used in single channel mode.

The speed is:

- 1 1/3 MHz in single channel mode (derived from CK/6-ØHT)
- 2 2/3 MHz in dual channel mode (derived from CK/3)

8.3.3.5 Data buffers

There are buffers D2121 and D2122 (partly) for display addresses, D2122 (partly) and D2123 for softkey text and D2124 for line text.

8.3.3.6 Address decoder

An address decoder D2132 is able to decode a number of addresses which are generated by the microprocessor.

This results in a number of signals (see also the preset sequence under section 8.3.2) according to the following table.

IOSL05LT	UPWR--LT	AB04	AB03	AB02	AB01	Output signal
0	0	1	0	0	0	WRDPSTLT
0	0	1	0	0	1	--
0	0	1	0	1	0	--
0	0	1	0	1	1	WRVEPOLT
0	0	1	1	0	0	WRHOPOLT
0	0	1	1	0	1	WRPSDPLT
0	0	1	1	1	0	WRDPPALT
0	0	1	1	1	1	WRHOVRLT

A chip select signal CSZ-CNLT for the Z-counter is generated via D2129 if IOSL05LT is active and AB04 is logic "0".

The signal overflow status can be read by the microprocessor via data bit DB00 (D2128-6), which is derived from signal DCDB10 via flip flop D2114. The overflow status (one or more bits in a display block) is read by the microprocessor after each display cycle.

8.3.3.7 Clock fase generator

A binary counter D2134 which can be resetted via the microprocessor reset signal UPRSOTLT counts the pulses from the 8 MHz microprocessor clocksignal DPCK08HT.

During each counter cycle, the counter is presetted to the value eleven when its fourth output bit is zero and a new clockpulse appears. The counter then continuous counting which results in the timing clock signals as shown in figure 8.3.6.

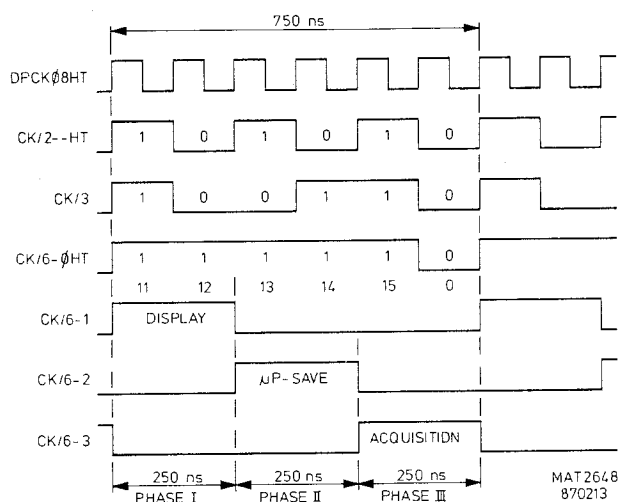


Figure 8.3.6 Clock signals.

8.3.3.8 Copy synchronization one-shot

The COPY SYNCHRONIZATION ONE-SHOT D2144 has no function in this instrument.

8.3.3.9 Memory select

The MEMORY SELECT circuit which mainly consists of the FPLA circuit D2151 generates a number of memory select, output enable and write enable signals.

8.3.3.10 Z-detection

The Z-DETECTION circuit which mainly consists of FPLS circuit D2142 generates one output signal Z-BL--HT which carries the blanking/unblanking information for the C.R.T. This signal is derived from a number of input conditions from a number of display circuits.

8.3.3.11 Z-timer

The Z-TIMER is for each block presettled with a value which is calculated by the microprocessor. The value depends on the total number of dots to be displayed during the actual display block. The counter starts counting down latch enable pulses LEDA--HT when enable display count signal ENDPCN is active. Until the end of the counting, when the zero state of the counter is reached, an output signal Z-DP is applied to the Z-DETECTION circuit. The C.R.T. trace can only be unblanked as long as the Z-TIMER is counting and signal Z-DP is generated.

8.3.3.12 Restart timer

This timer especially has a function when X-EXPAND is selected and is for each block presettled with a value which is calculated by the microprocessor. The value depends on the X-EXPAND factor and the total number of dots to be displayed during the actual display block.

If for example the X-EXPAND factor is *4, the display block will be displayed four times in order to reach a same trace intensity on the C.R.T. screen as there is without X-expansion.

After the first display action, when the zero state of the restart timer is reached, and restart display signal RDDP--LT is generated to start the second display action and so on. After display action four (in this example) the end of the complete display block is given by the IL05--LT output signal from the interrupt timer.

8.3.3.13 Interrupt timer + flip flop

This timer is for each display block presettled with a value which is calculated by the microprocessor. The value depends on the total number of dots to be displayed during the actual display block. The counter starts counting down latch enable pulses LEDA--HT when enable display count signal ENDPCN is active. At the end of the counting, when the zero state of the counter is reached, an output signal is applied to the interrupt flip flop D2133 and an interrupt signal IL05--LT for the microprocessor is generated to indicate the end of the actual display cycle.

8.3.3.14 Start + smooth delay flip flop

The START flip flop is blocked by signal IL05DPLT on input 11 as long as a display preset sequence is performed. At the end of such a sequence a display start signal WRDPSTLT is generated and the start flip flop D2127 produces a 3 us start signal STDP. This STDP signal is applied to the synchronization flip flop D2114 to start the display of a new block.

A new display action can also be started via a RTDP--LT output pulse from the restart-timer.

If SMOOTH is selected, an additional delay of 12 us is introduced by smooth delay flip flop D2127 and a smooth delay signal SMDL--LT is then applied to synchronization flip flop D2116. This is done at the end of a sweep to avoid connection of the last dot of a sweep with the first one of the next sweep.

NOTE: In this instrument the smooth circuit is not activated.

8.3.3.15 Plot one-shot

If a plot function is selected (signal PLOT active) the plot one-shot D2144 will generate a sample plot pulse SAPL for the analog plot interface on unit A1 at the beginning of the plot block. This is the last block of a display cycle.

In this way one dot per display cycle can be plotted. The minimum plot time is therefore 20 ms/dot. Slower plot speeds can be selected via the PLOT menu.

The microprocessor knows how many dots have to be plotted and which actual dot has to be plotted. The memory address of the actual dot to be plotted, is presetted in the display address counter and the data which is stored in this address location is applied to the plot interface on unit A1.

The penlift (pen up/pen down) can be controlled via the microprocessor generated signal PU---LT.

The polarity of the penlift is also generated by the microprocessor by generating signal PFPY.

If the Z-signal is blanked (during overscan for example) the pen is also lifted automatically.

If no plot function is selected, the plot outputs are short circuited via signal PLZEOT.

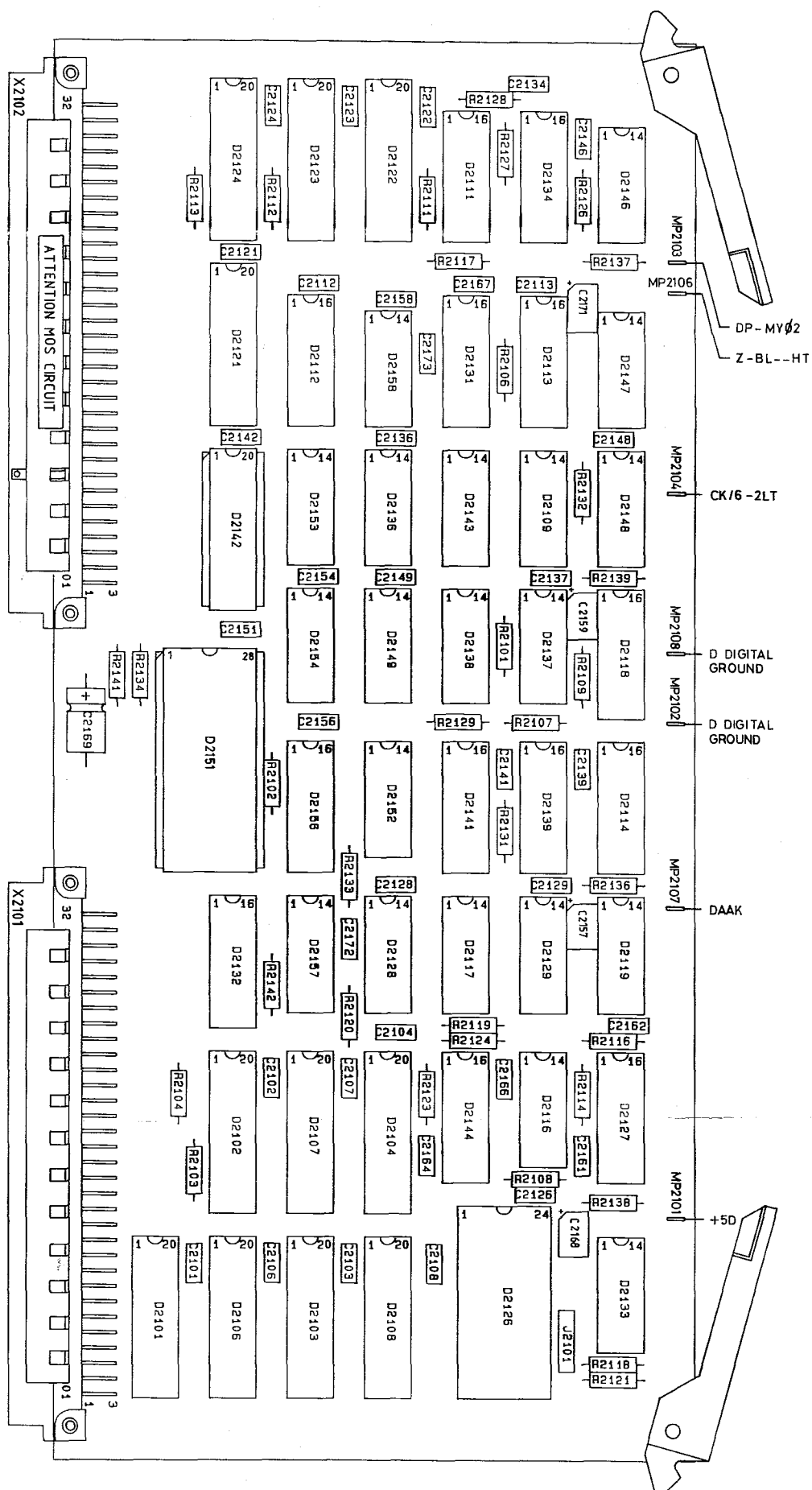
8.3.4 Signal-name list

UNIT A3

Signal-name	Description	Signal source	Signal destination(s)
AB01...15	Address bus 01...15	A6+Option	-
ANCPY-HT	Analog compress Y	A3	A12-A1
ANEPY-HT	Analog expand Y	A3	A12-A1
BUAB13...15	Buffered address lines 13...15	A3	A3
BUHISBLT	Buffered high strobe	A3	A3
BULOSBLT	Buffered low strobe	A3	A3
CHID	Channel indentification	A3	A3
CKEPVE	Clock expand vertical	A3	A12-A2
CKSVLA	Clock save latch	A3	A12-A4
CK/2--LT	Clock /2	A3	A3
CK/2--HT	Clock /2	A3	A3
CK/3	Clock /3	A3	A3
CK/6-0LT	Clock /6-0	A3	A3
CK/6-0HT	Clock /6-0	A3	A3
CK/6-1LT	Clock /6-1	A3	A3
CK/6-1HT	Clock /6-1	A3	A3
CK/6-2LT	Clock /6-2	A3	A3
CK/6-2HT	Clock /6-2	A3	A3
CLDPAB	Clock display address bus (CK/6-1HT)	A3	A12-A4
CLUPAB	Clock microprocessor bus (MMYSL02HT)	A3	A12-A4
CSTX--LT	Chip select text	A3	A12-A4
CSZ-CNLT	Chip select Z-counter	A3	A3
DAAK--LT	Data acknowledge	A3	A12-A4
DAAK--HT	Data acknowledge	A3	A12-A4
DAHISBLT	Data high strobe	A6+Option	-
DALOSBLT	Data low strobe	A6+Option	-
DATRAKLT	Data trace acknowledge	A3+A5+A6+A8+Option	A12-A6, A12-Option
DB00...15	Data bus 00...15	A6+Option	-
DCDB09...15	Display control data bus 09...15	A4	-
DIDBTX	Disable data bus text-buffer	A3	A12-A4
DIDJ	Disable dot join	A3	A3
DIDPCN	Disable display counter	A3	A3
DIDPPS	Disable display preset	A3	A3
DIOS--HT	Disable overscan	A3	A12-A1, A12-A2
DISVLA	Disable save latch	A3	A4
DITXTR	Disable text trace buffer	A3	A12-A4
DJAC--HT	Dot join active	A3	A12-A2
DPAB00...11	Display address bus 00...11	A3	A12-A4
DPCK08LT	Display clock 8 Mhz	A3	A3
DPCK08HT	Display clock 8 Mhz	A3	A3
DPCNCK	Display counter clock	A3	A3
DPDB00...15	Display data bus 00...15	A3	A3
DPMO--LT	Display mode	A3	A3

Signal-name	Description	Signal source	Signal destination(s)
DPMYRDHT	Display memory read	A3	A3
DPMYWRHT	Display memory write	A3	A3
DPMY00...02	Display memory 00...02	A3	A3
DPMY02LT	Display memory 02	A3	A3
DPRJUPLT	Display reject up	A3	A12-A2
DPRJDWLT	Display reject down	A3	A12-A2
DRTXTR	Direction text trace buffer	A3	A12-A4
DPTR--HT	Display trace (DPMY02LT)	A3	A12-A1
ENDPCN	Enable display counter	A3	A3
ENTRHOLT	Enable trace horizontal	A3	A12-A2
ENTRHOHT	Enable trace horizontal	A3	A3
ENTXLNLT	Enable text line	A3	A12-A2
ENTXSKLT	Enable text softkey	A3	A3
EPDB00...11	Expanded data bus	A2,A3	A12-A2
EPHO14	Expanded horizontal bus 14	A3	A12-A2
EPX-00...02	Expand X 00...02	A3	A12-A2
EPY-00...01	Expand Y 00...01	A3	A12-A2
EP12--LT	Expand 12	A3	A12-A2
HOMO	Horizontal mode	A3	A3
IL05--LT	Interrupt level 05	A3	A12-A6
IL05DPLT	Interrupt level 05 display	A3	A3
IOSL05LT	I/O select 05	A6	-
IVDCDB	Invert display control address bus	A3	A12-A2
LEDA--LT	Latch enable DAC	A3	A12-A2
LEDA--HT	Latch enable DAC	A3	A12-A2
LEDC	Latch enable display control	A3	A12-A4
MXCPAD (WRAQ--HT)	Multiplex copy address	A3	A12-A4
MYSL02LT	Memory select 02	A6+Option	-
MYSL02HT	Memory select 02 (CLUPAB)	A3	-
OETR01LT	Output enable trace 01	A3	A12-A4
OETR02LT	Output enable trace 02	A3	A12-A4
OETX--LT	Output enable text	A3	A12-A4
PFPY	Penlift polarity	A3	A12-A1
PLOT	Plot	A3	A3
PLZEOT	Plot zero output	A3	A12-A1
PSDP00...11	Present display bus 00...11	A3	A3
PU---LT	Pen-up signaal	A3	A12-A1
RDDM--LT	Read display memory	A3	A12-A4
RDDPDALT	Read display data	A3	A3
RSDAAKLT	Reset data acknowledge	A3	A3
RTDP--LT	Restart display	A3	A3
SAPL	Sample plot	A3	A12-A1
SAPL--LT	Sample plot	A3	A3
SARY	Sample ready	A4	-
SARYAKLT	Sample ready acknowledge (DITRDB) (WRAQ--RT)	A3	A12-A4

Signal-name	Description	Signal source	Signal destination(s)
SAVE---LT	Save	A3	A3
SLTR1LLT	Select trace 1L	A3	A12-A4
SLTR1HLT	Select trace 1H	A3	A12-A4
SLTR2LLT	Select trace 2L	A3	A12-A4
SLTR2HLT	Select trace 2H	A3	A12-A4
SM----LT	Smooth	A3	A12-A2
SMDL--LT	Smooth delay	A3	A3
STDP	Start display	A3	A3
SVR1	Save register R1	A3	A3
SVR2--LT	Save register R2	A3	A3
SVR3	Save register R3	A3	A3
SYDP	Synchronize display	A3	A12-A8
TRAB13	Trace address bus 13	A3	A12-A4
TXAB13	Text address bus 13	A3	A12-A4
TXLNSKLT	Text line softkey	A3	A3
UPCK08	Microprocessor clock 8 Mhz	A6	-
UPRD--LT	Microprocessor read	A6	-
UPRD--HT	Microprocessor read	A3	A3
UPRSOTLT	Microprocessor reset out	A6	-
UPWR--LT	Microprocessor write	A6	-
VEDB09...12	Vertical data bus 09...12	A2	-
WETR01LT	Write enable trace 01	A3	A4
WETR02LT	Write enable trace 02	A3	A12-A4
WETX--LT	Write enable text (WR02--LT)	A3	A12-A4
WRAQ--LT	Write acquisition	A3	A3
WRAQ--HT	Write acquisition (SARYAKLT)	A3	A3
WRDPPALT	Write display parameters	A3	A3
WRDPSTLT	Write display start	A3	A3
WRHOPOLT	Write horizontal position	A3	A12-A2
WRHOVRLT	Write horizontal variable	A3	A12-A2
WRPSDPLT	Write preset display	A3	A3
WRVEPOLT	Write vertical position	A3	A12-A2
WR00--LT	Write 00	A3	A3
WR01--LT	Write 01	A3	A3
WR02--LT	Write 02 (WETX--LT)	A3	A12-A4
Z-AC--LT	Z - active	A3	A3
Z-BL--HT	Z - blanking signal	A3	A12-A1
Z-DP	Z - display	A3	A3
Z-OT03	Z - output 03	A2	-



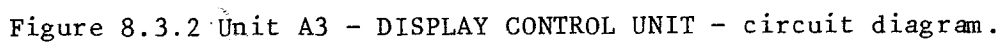
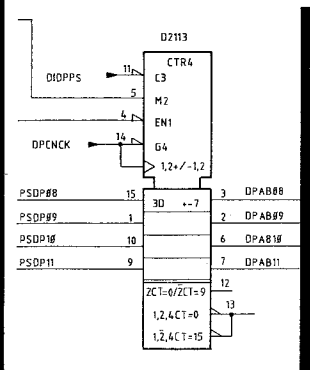
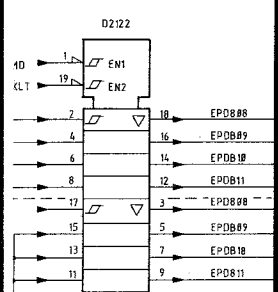
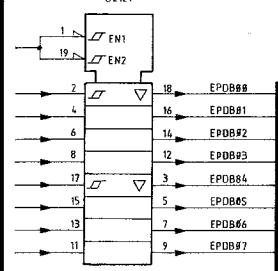


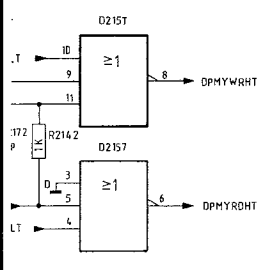
Figure 8.3.2 Unit A3 - DISPLAY CONTROL UNIT - circuit diagram.



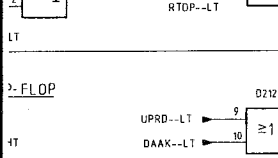
ADDRESS DATA BUFFER
D2121



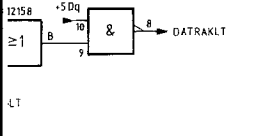
SOFTKEY TEXT DATA BUFFER
D2122



SOFTKEY TEXT DATA BUFFER
D2127

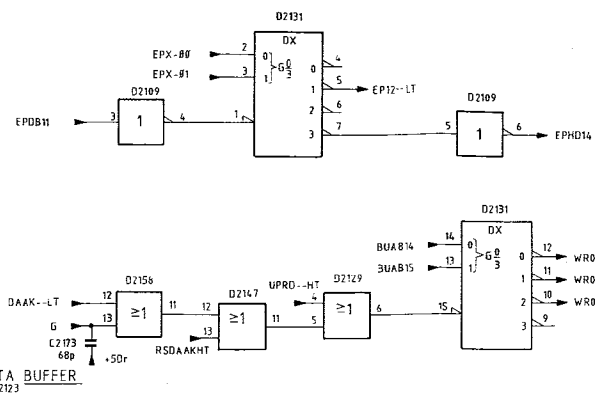


START FLIP-FLOP
D2127

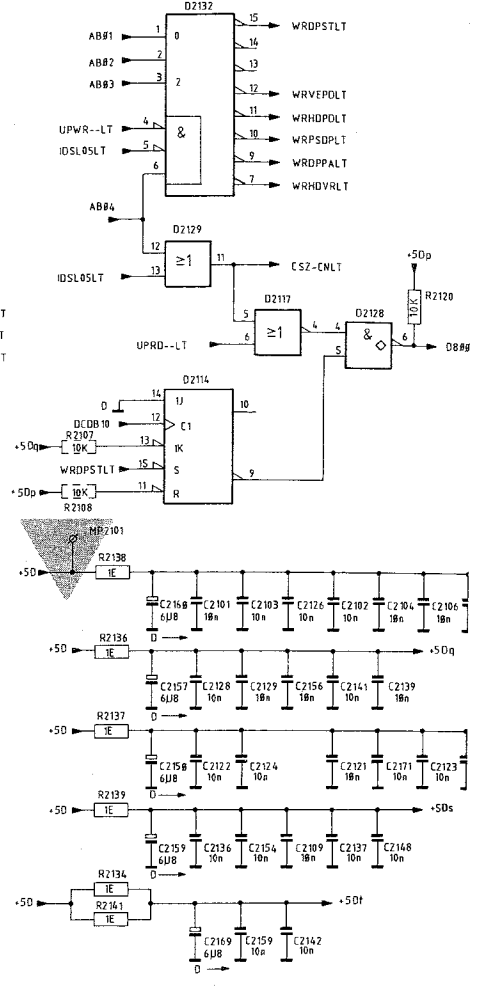


SMOOTH DELAY FLIP-FLOP
D2127

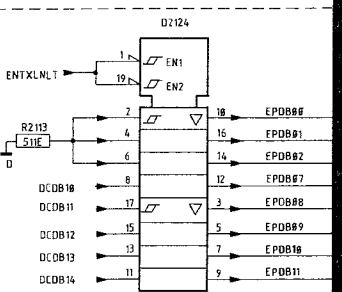
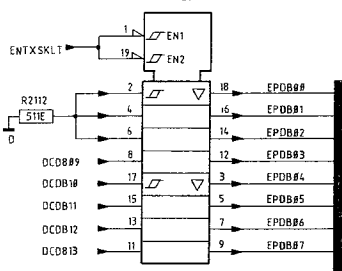
HORIZONTAL EXPAND I (PART)



ADDRESS DECODER

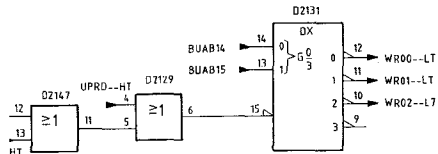
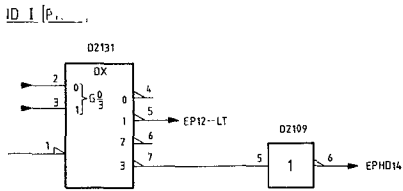


SOFTKEY TEXT DATA BUFFER
D2123



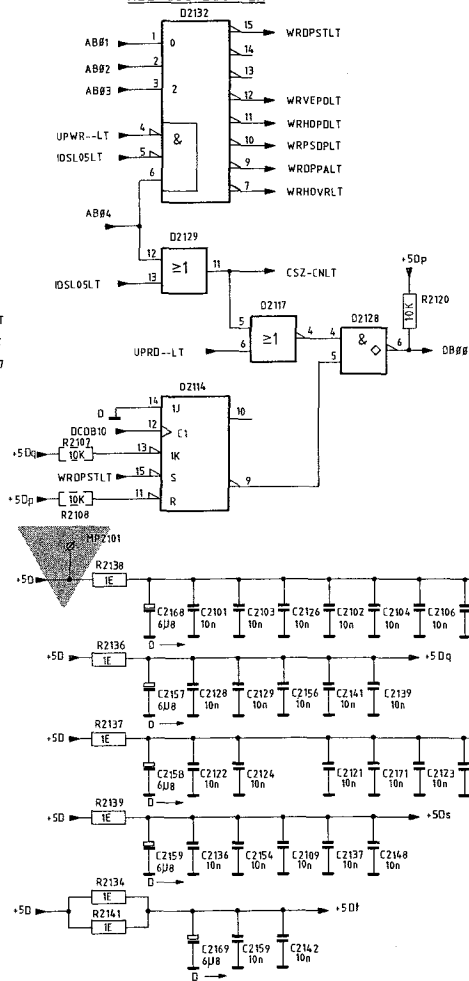
LINE TEXT DATA BUFFER
D2124

REF NR	TYPE	V _{CC}	PEN	V _{DD}	PEN
D2103,2104,2106,2107,2108	74HCT574	+50p	20	D	10
D2158	74 F 32	+50p	16	D	7
D2196	74F04	+50p	16	D	7
D2156	74HCT174	+50p	16	D	8
D2157	74HCT127	+50p	16	D	7
D2133	74HCT107	+50p	16	D	7
D2147	74 F 52	+50p	16	D	7
D2137	74HCT132	+50p	16	D	7
D2138	74HCT108	+50p	16	D	7
D2111,2112,2113	74HCT191	+50p	16	D	8
D2171,2172,2173,2174	74HCT124	+50p	28	D	10
D2132	74HCT138	+50p	16	D	8
D2131	74HCT139	+50p	16	D	8
D2146	74HCT127	+50p	16	D	7
D2139,2141	74F109	+50p	16	D	8
D2114	74HCT109	+50p	16	D	8
D2109	74F04	+50p	16	D	7
D2118	74HCT257	+50p	16	D	8
D2119	74HCT108	+50p	16	D	7
D2143	74HCT08	+50p	16	D	7
D2154	74F04	+50p	14	D	7
D2129	74HCT132	+50p	16	D	7
D2117	74HCT162	+50p	16	D	7
D2116	74HCT174	+50p	16	D	7
D2101,2102	74HCT241	+50p	20	D	10
D2148	74F74	+50p	16	D	7
D2127,2144	74HCT123	+50p	16	D	8
D2128	74LS38	+50p	16	D	7
D2153	74 F 11	+50p	15	D	7
D2126	P0254	+50p	24	D	14
D2134	74F163	+50p	16	D	8
D2152	74F32	+50p	14	D	10
D2142	S155	+50p	20	D	10
D2151	S100	+50p	28	D	14
D2149	74F08	+50p	14	D	7



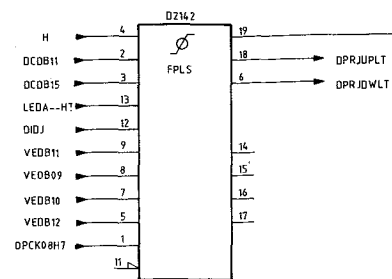
- EPD008
- EPD001
- EPD002
- EPD003
- EPD004
- EPD005
- EPD006
- EPD007
- EPD008
- EPD009
- EPD010
- EPD011

ADDRESS DECODER

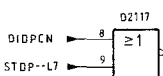


Z-AC--LT
Z-OP
Z-DT03

Z-DETECTION

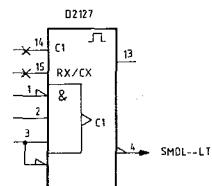


PLOT ONE-SHOT



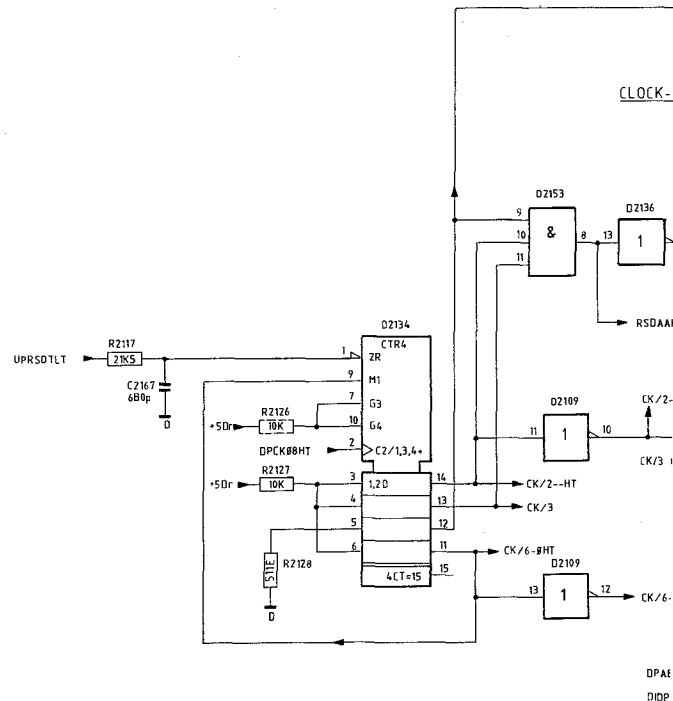
COPY SYNCHRONIZATION ONE-SHOT

SMOOTH-DELAY FLIP-FLOP



MAT 25 87A

REF.NR.	TYPE	TRC	PEN	Vdd	PEN
D2103, 2104, 2106, 2107, 2108	74HCT574	+50p	20	D	10
D2158	74 F 32	+50p	14	D	7
D2136	74F04	+50p	14	D	7
D2156	74HCT174	+50p	16	D	8
D2157	74HCT127	+50p	14	D	7
D2133	74HCT107	+50p	14	D	7
D2147	74 F 32	+50p	14	D	7
D2137	74HCT132	+50p	14	D	7
D2138	74HCT108	+50p	14	D	7
D2111, 2112, 2113	74HCT191	+50p	16	D	8
D2121, 2122, 2123, 2124	74HCT244	+50p	20	D	10
D2132	74HCT138	+50p	16	D	8
D2131	74HCT139	+50p	16	D	8
D2146	74HCT127	+50p	14	D	7
D2139, 2141	74F09	+50p	16	D	8
D2114	74HCT109	+50p	16	D	8
D2109	74F04	+50p	14	D	7
D2118	74HCT1257	+50p	16	D	8
D2119	74HCT108	+50p	14	D	7
D2143	74HCT00	+50p	14	D	7
D2154	74F00	+50p	14	D	7
D2129	74HCT132	+50p	14	D	7
D2117	74HCT102	+50p	14	D	7
D2116	74HCT114	+50p	14	D	7
D2101, 2102	74HCT541	+50p	20	D	10
D2148	74F74	+50p	14	D	7
D2127, 2144	74HCT123	+50p	16	D	8
D2128	74LS38	+50p	14	D	7
D2153	74 F 31	+50p	14	D	7
D2126	P8254	+50p	24	D	14
D2134	74F163	+50p	16	D	8
D2152	74F32	+50p	14	D	7
D2147	S155	+50p	20	D	10
D2151	S100	+50p	28	D	14
D2149	74F08	+50p	14	D	7



DPAE
DIDP

