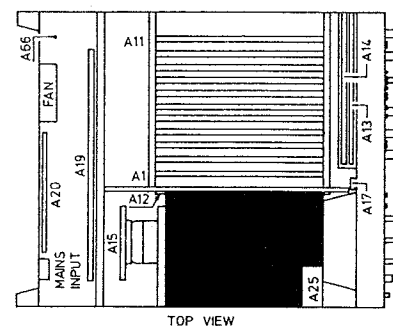


UNIT A25 - MANAGEMENT UNITCONTENTS

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8.25.1 General information

This unit mainly consists of:

- an interface between the microprocessor (unit A6) and the signal acquisition units (A31, A32, A34, A51 and A52).
- the first part of feedback loop.
- some auxiliar circuits.

8.25.2 Interface

The interface part consists of:

DATA BUFFER	D3101
ADDRESS BUFFER	D3102
I/O SELECT DELAY	D3117, D3119
ADDRESS DECODER	D3104, D3106, D3107
STATUS FLIPFLOPS	D3108, D3109, D3111, D3112, D3113, D3114, D3116
INPUT PORT	D3103
OFFSET DACs	D3136, D3137, D3138, D3139
TRIGGER LEVEL DAC	D3141

Data from or to the microprocessor are buffered by the bidirectional DATA BUFFER.

The ADDRESS BUFFER buffers four address lines (AB01...AB04) from the microprocessor before they are applied to the ADDRESS DECODER. It also buffers some control signals.

The I/O SELECT DELAY generates correctly timed signals to control the buffers.

The ADDRESS DECODER generates clock signals for the STATUS FLIPFLOPS and 4 latch enable signals for DACs on this unit and the Time-base unit A51. These signals are: LETRLV, LETRDL, LEHDOF and LEFSRM.

The latch enable signal for the INPUT PORT is generated at D3104 pin 14.

The STATUS FLIPFLOPS generate a number of latch enable signals for serial latches, and data plus clock signals for these latches (SEDA1, SEDA2, SECK1 and SECK2).

The latch enable signals are:

Name	Destination
LEVGBA	Management unit A25
LEVGBB	Management unit A25
LEVGBA	Vertical signal unit A55
LEVGBB	Vertical signal unit A55
LEVEA	Vertical signal unit A55
LEVEB	Vertical signal unit A55
LETRST	Trigger control unit A34
LETBST	Time-base unit A51

If a setting modification of the instrument means that a new acquisition should be started, then the new setting is done via SEDA1 and SECK1 (e.g. TRIGGER LEVEL), otherwise it is done via SEDA2 and SECK2 (e.g. OFFSET).

Via the INPUT PORT the microprocessor reads four probe information signals from the Distribution unit A53 and three signals from the Trigger control unit A34.

The four OFFSET DACs are 14 bit serial DACs. Two DACs give an offset coarse signal (one for each channel) and the other two DACs give an offset fine signal. The four output signals are applied to the Vertical signal unit A55.

The TRIGGER LEVEL DAC is also a 14 bit serial DAC. Its output signal is applied to the Trigger control unit A34.

8.25.3 Feedback loop

The part of the feedback loop that is mounted on this unit consists of twice the same circuit, one for each channel. Only the part from channel A will be described.

The sample data from the DPU unit A9 are stored in the SAMPLE DATA REGISTER (D3122, D3123). The most significant dataline SADB11 is inverted in CODE CONVERT to obtain conversion from two's complemented code to straight binary code.

When FBRY goes high the sample data are stored. The signal CHPTdetermines whether the sample data are for channel A (high) or for channel B (low).

The sample data are converted into an analog voltage by the FEEDBACK DAC (D1327) and two opamps (N3129, N3131) and associated circuitry. This voltage is applied to a multiplying DAC (D3143) of the VARIABLE FEEDBACK circuit. The digital code to the DAC comes from a shift register (D3142), which gets its data from the microprocessor. The output signal of the DAC is buffered and applied to the Vertical signal unit A55.

8.25.4 Auxiliar circuits

The CHANNEL SWITCH DRIVER converts the channel switch signal (CHSW) in a current (CHSW-1) which is able to drive the CHANNEL SWITCH on the Vertical signal unit A55.

NOTE: The flatcable between connector X501 on the Motherboard unit A12 and connector X3101 on this unit has crossed interconnections. This means that connector pin A1 on one end becomes B32 on the other end, etc.

8.25.5 Signal name list

UNIT 25

Signal name	Description	Signal source	Signal destination(s)
AB01...04	Address bus 01...04	A6+Option	-
AB01-1...04-1	Address bus 01-1...04-1	A25	A25
CHPT	Channel pointer	A5	-
CHSW	Channel switch	A5	-
CHSW-1	Channel switch 1	A25	A53-A55
CKVEA	Clock vertical A	A25	A25
CKVEB	Clock vertical B	A25	A25
CKACL	Clock acquisition control logic	A25	A25
CKSEDA	Clock serial data	A25	A25
CKTB	Clock time-base	A25	A25
CKTR	Clock trigger	A25	A25
CKVGBA	Clock variable gain backward A	A25	A25
CKVGBB	Clock variable gain backward B	A25	A25
CKVGFA	Clock variable gain forward A	A25	A25
CKVGFB	Clock variable gain forward B	A25	A25
CNDWMO	Count down mode	A34	-
CNSTCNLT	Count stair counter	A5	-
DB08...15	Data bus 08...15	A6+Option	-
DB08-1...15-1	Data bus 08-1...15-1	A25	A25
FBOTA	Feedback output A	A25	A25
FBOTB	Feedback output B	A25	A25
FBRY	Feedback ready	A8	-
IOSL07LT	I/O select 07	A6	-
IOSL07-1	I/O select 07-1	A25	A25
LEACL	Latch enable acquisition control logic	A25	A12-A5
LEFSRM	Latch enable fast ramp	A25	A53-A51
LEHDOF	Latch enable hold off	A25	A53-A51
LETBST	Latch enable time-base status	A25	A53-A51
LETRDL	Latch enable trigger delay	A25	A53-A51
LETRLV	Latch enable trigger level	A25	A25
LETRST	Latch enable trigger status	A25	A53-A51-A34
LEVEA	Latch enable vertical A	A25	A53-A55
LEVEB	Latch enable vertical B	A25	A53-A55
LEVGBA	Latch enable variable gain backward A	A25	A25
LEVGBB	Latch enable variable gain backward B	A25	A25

Signal name	Description	Signal source	Signal destination(s)
LEVGF A	Latch enable variable gain forward A	A25	A53-A55
LEVGF B	Latch enable variable gain forward B	A25	A53-A55
LOSCRA	Latch offset coarse A	A25	A25
LOSCRB	Latch offset coarse B	A25	A25
LOSFIA	Latch offset fine A	A25	A25
LOSFIB	Latch offset fine B	A25	A25
OSCR A	Offset coarse A	A25	A55
OSCR B	Offset coarse B	A25	A55
OSFIA	Offset fine A	A25	A55
OSFIB	Offset fine B	A25	A55
PRIFA1	Probe information A1	A53	-
PRIFA2	Probe information A2	A53	-
PRIFB1	Probe information B1	A53	-
PRIFB2	Probe information B2	A53	-
RDPRIF	Read probe information	A25	A25
RSSTCNLT	Reset stair counter	A5	-
SADB00...10	Sample data bus 00...10	A9+A11	-
SECK1	Serial clock 1	A25	A25, A53-A55, A53-A51, A53-A51-A34
SECK2	Serial clock 2	A25	A25, A53-A55, A53-A51
SEDA1	Serial data 1	A25	A25, A53-A55, A53-A51, A53-A51-A34
SEDA2	Serial data 2	A25	A25, A53-A55, A53-A51
STSAGTLT	Start sampling gate	A52	-
SYMO--LT	Synchronize mode	A34	-
TRLV	Trigger level	A25	A34
TRSVHI	Trigger sensitivity high	A34	-
UPRD--LT	Microprocessor read	A6	-
UPRD-1LT	Microprocessor read 1	A25	A25
UPRSOT-1	Microprocessor reset output 1	A25	A25
UPRSOTLT	Microprocessor reset out	A6	-
UPWR--LT	Microprocessor write	A6	-
UPWR-1LT	Microprocessor write 1	A25	A25
VBOTA	Variable backward output A	A25	A55
VBOTB	Variable backward output B	A25	A55
VGDA00...11	Variable gain data A 00...11	A25	A25
VGDB00...11	Variable gain data B 00...11	A25	A25

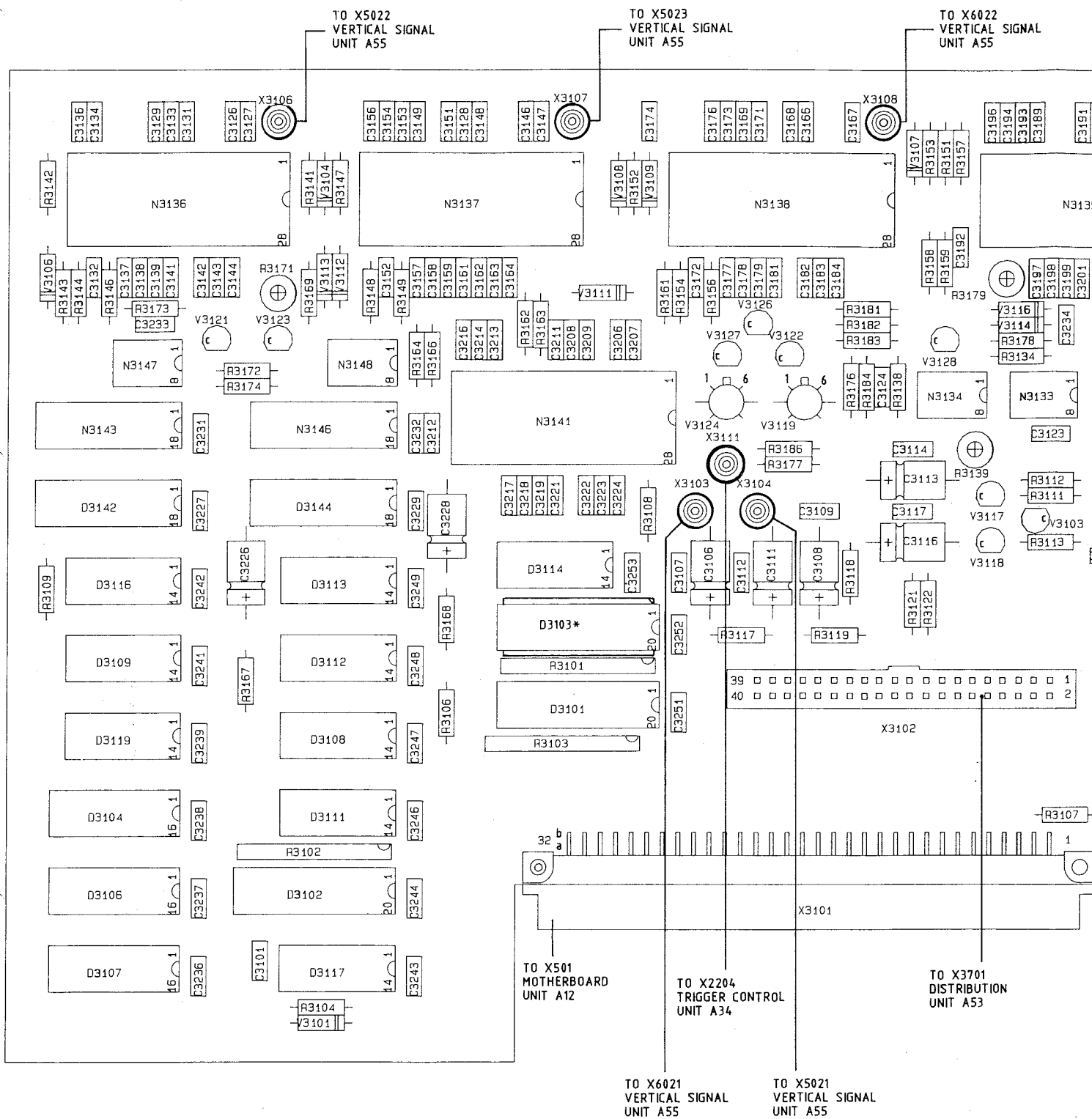
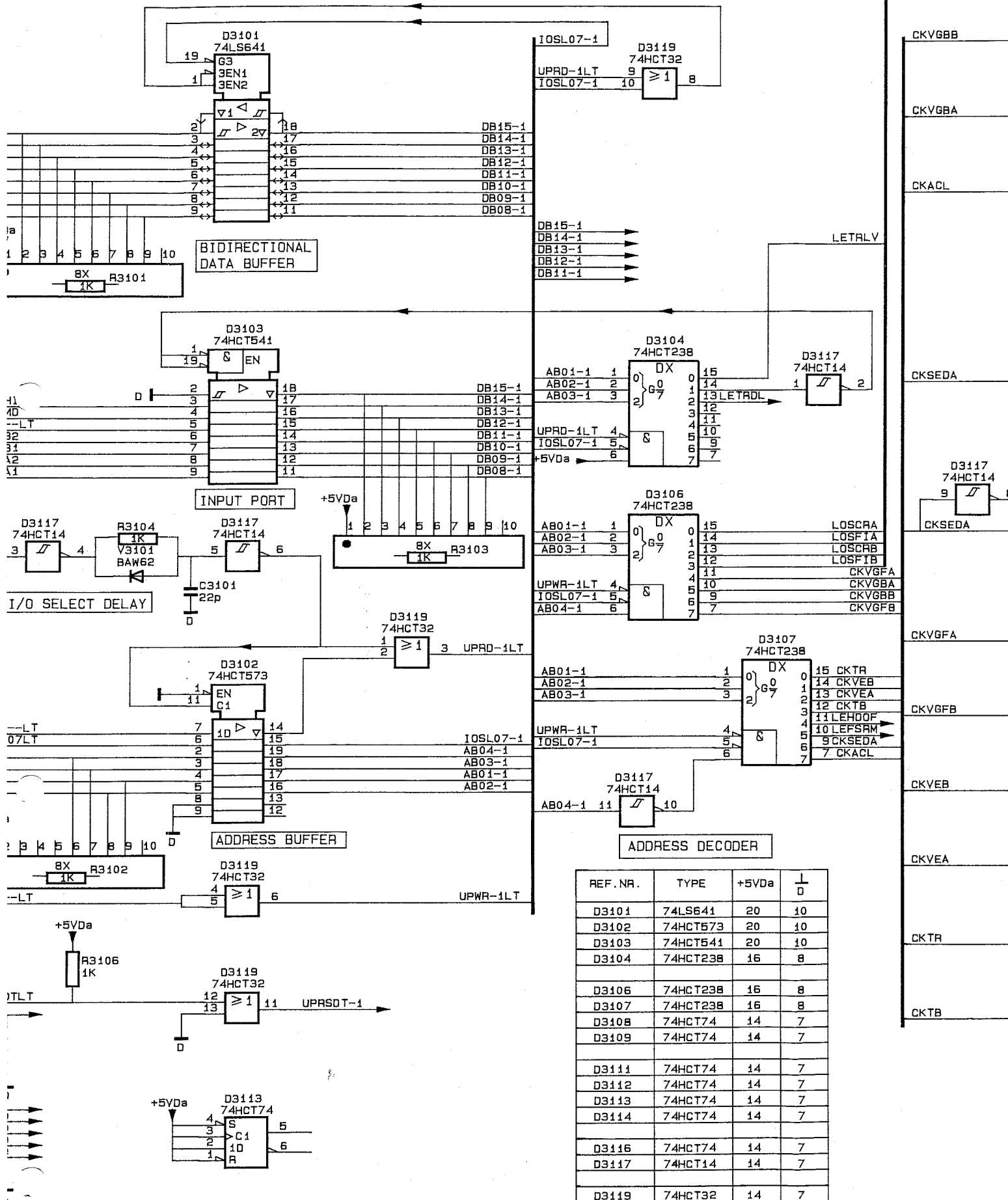
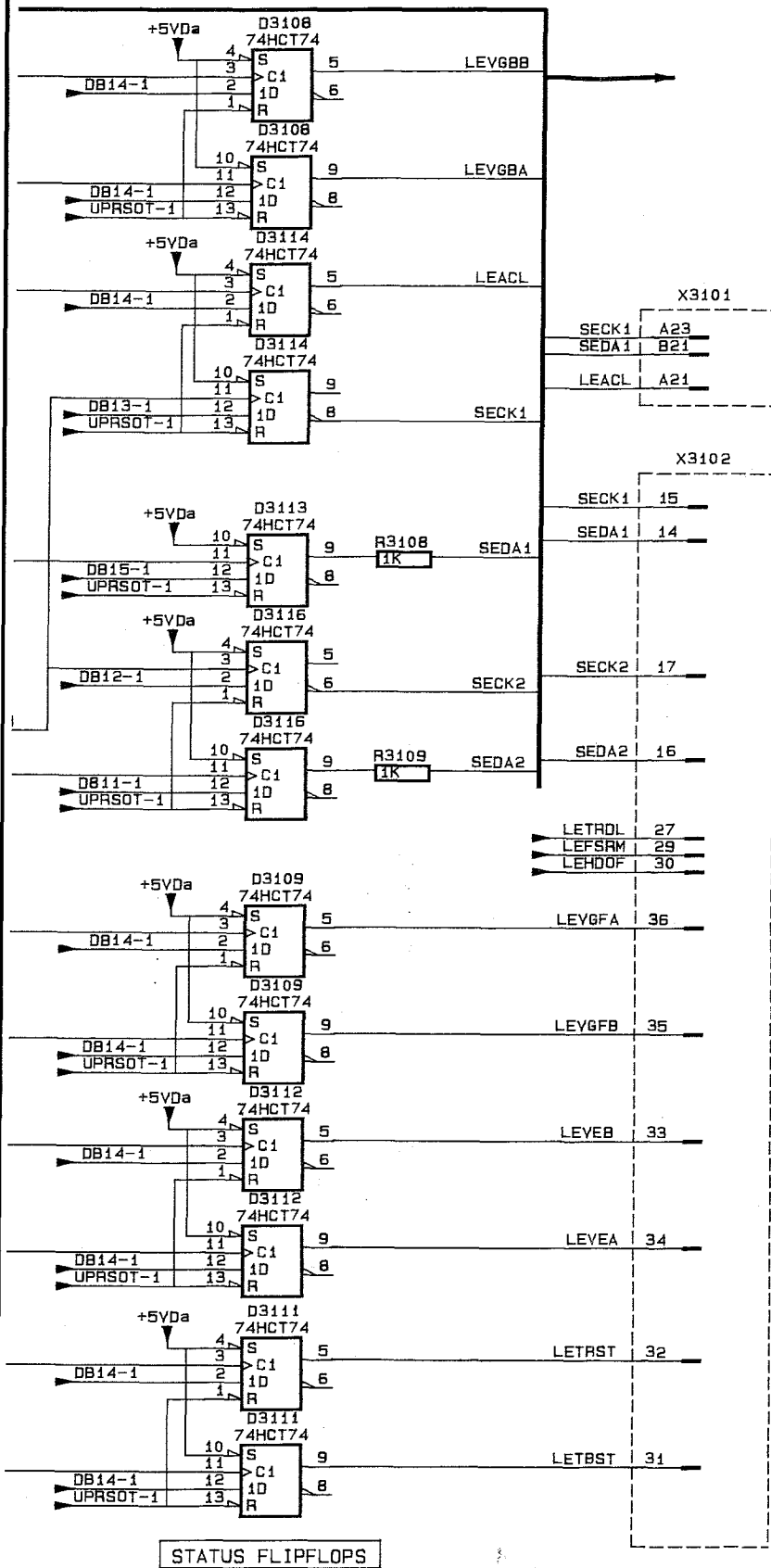


Figure 8.25.1 Unit A25 - MANAGEMENT UNIT - p.c.b. lay-out.



Unit A25 - MANAGEMENT UNIT - circuit diagram.



MAT 3250

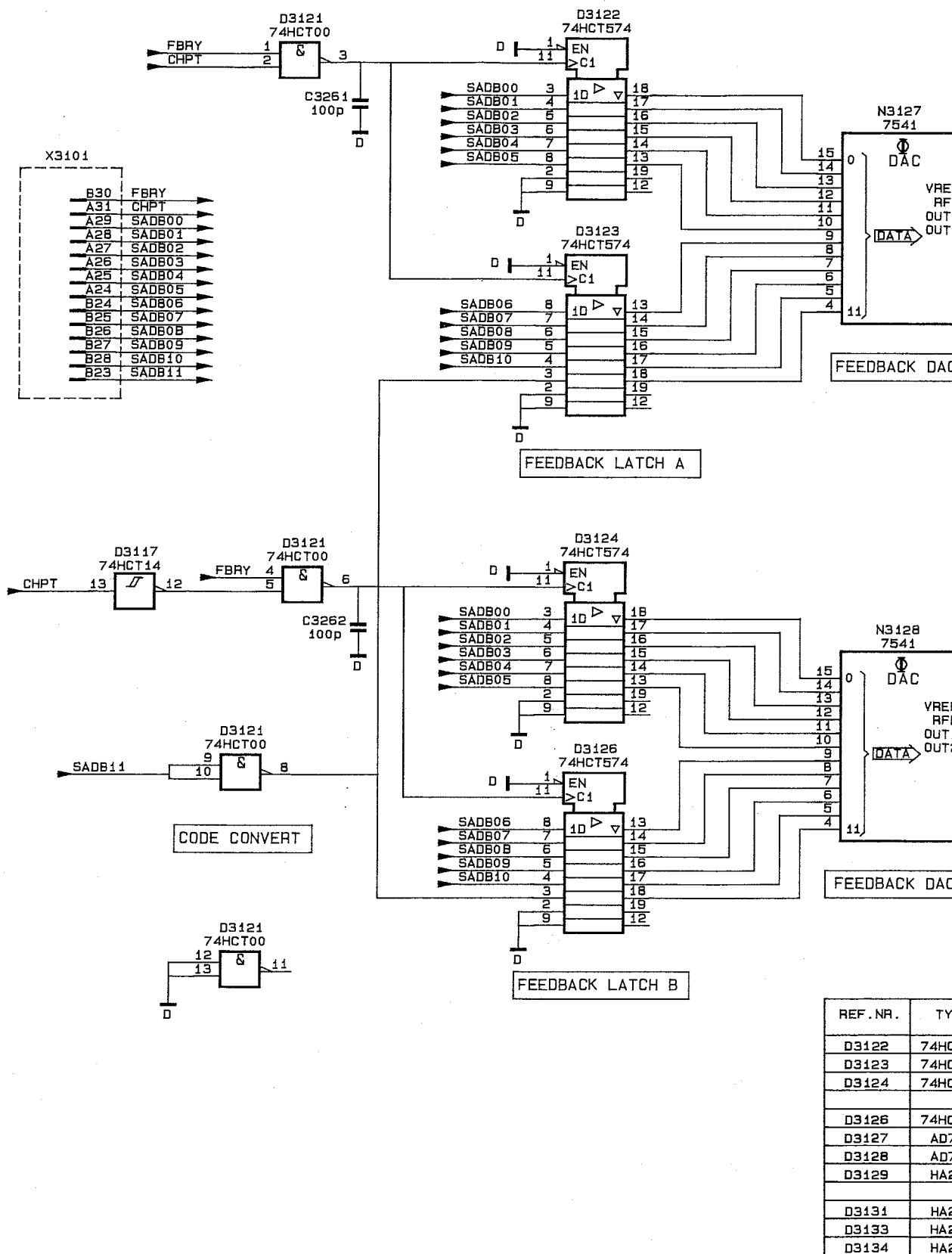
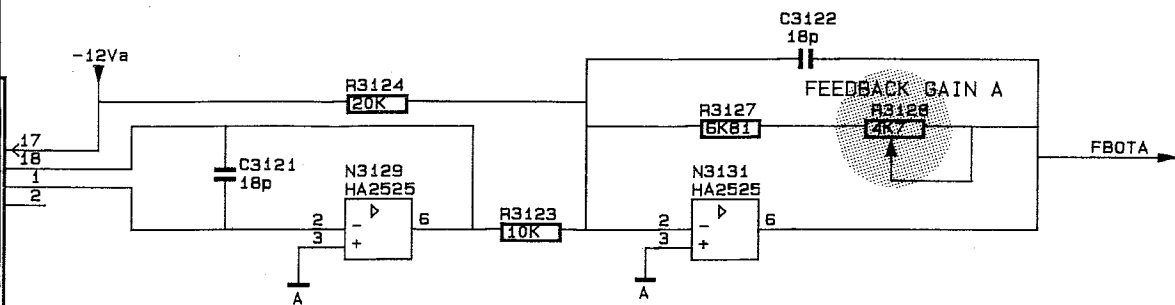
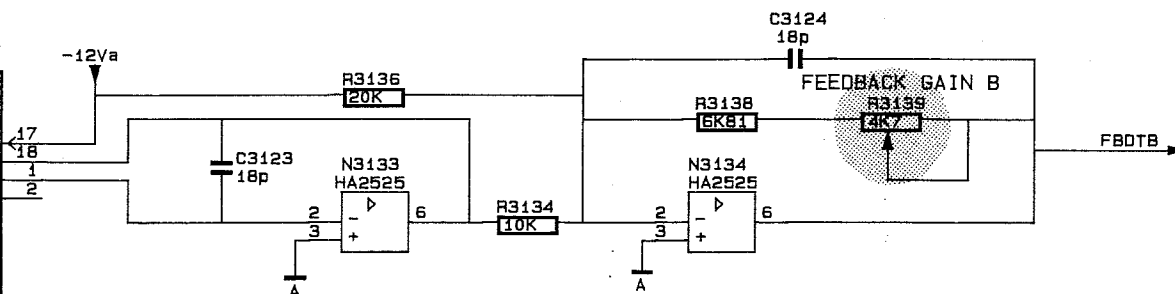


Figure 8.25.3 Unit A25 - MANAGEMENT UNIT - circuit diagram.



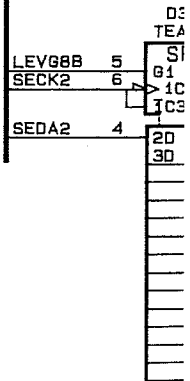
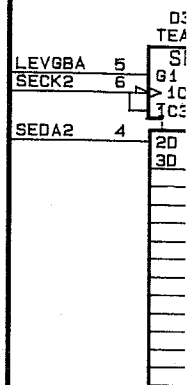
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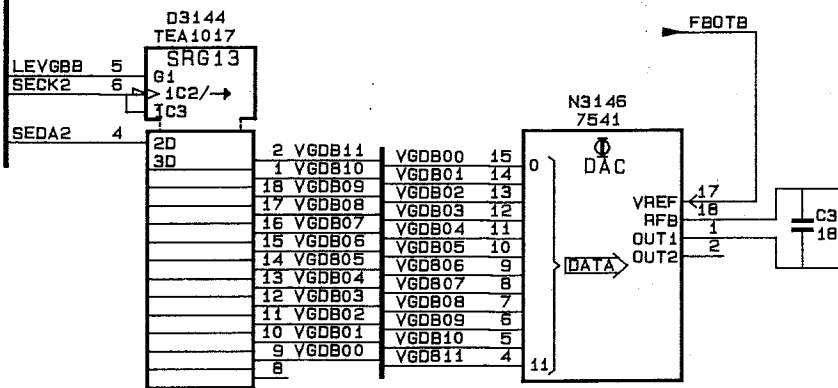
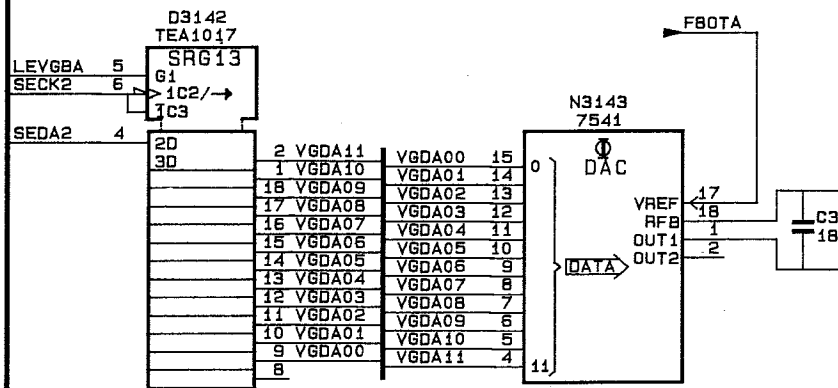
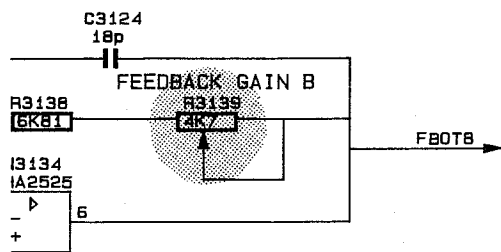
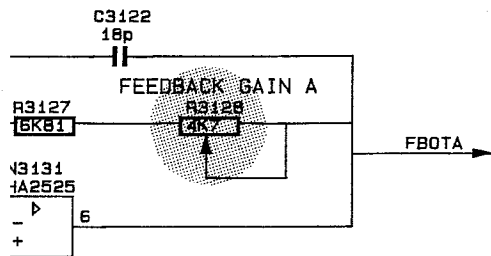


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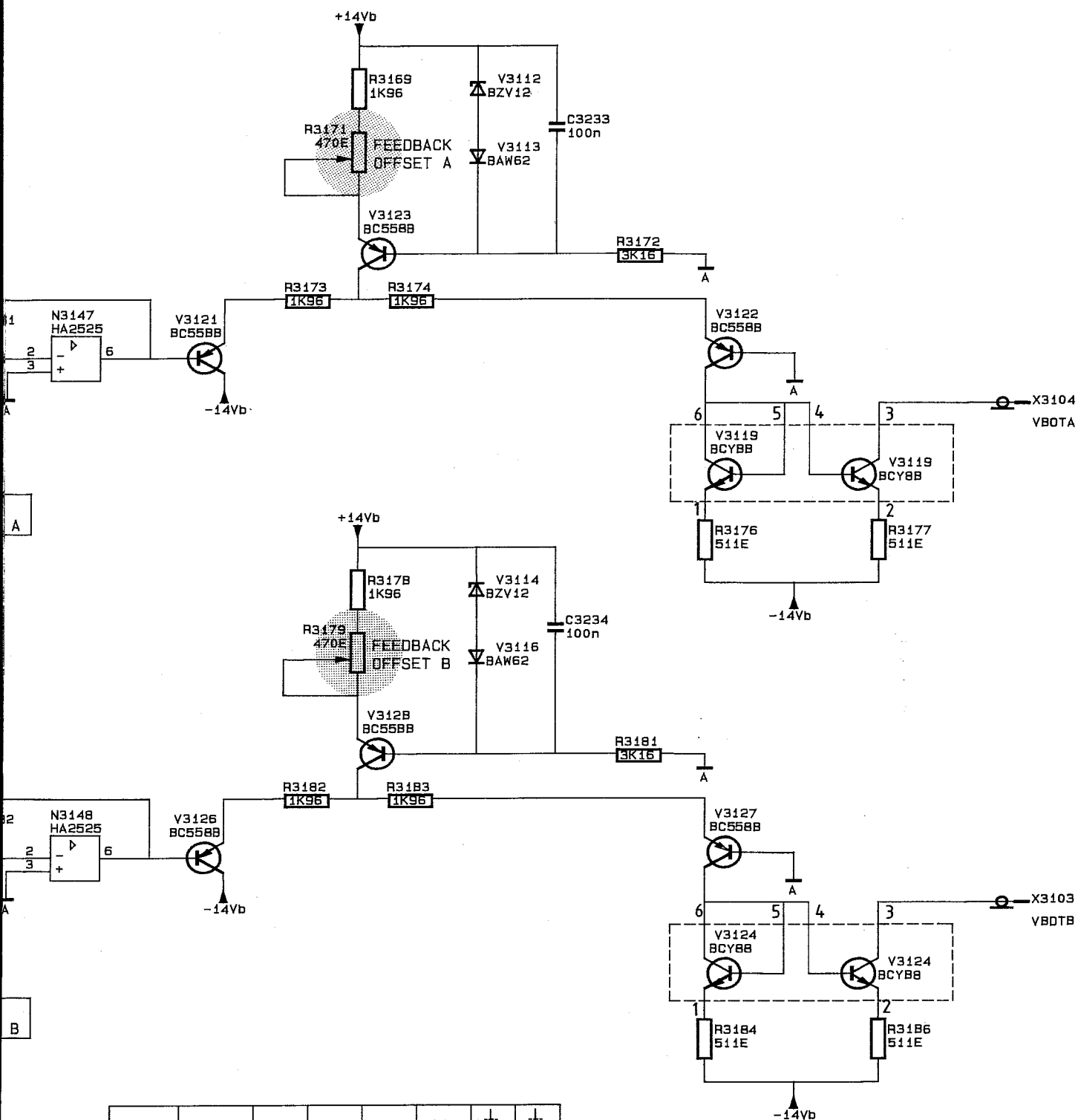
E	+5Vda	+14Vb	-14Vb	$\frac{1}{A}$	$\frac{1}{D}$
574	20				10
574	20				10
574	20				10
574	20				10
541		16		3	
541		16		3	
525		7	4		
525		7	4		
525		7	4		
525		7	4		

I
MAT 3251



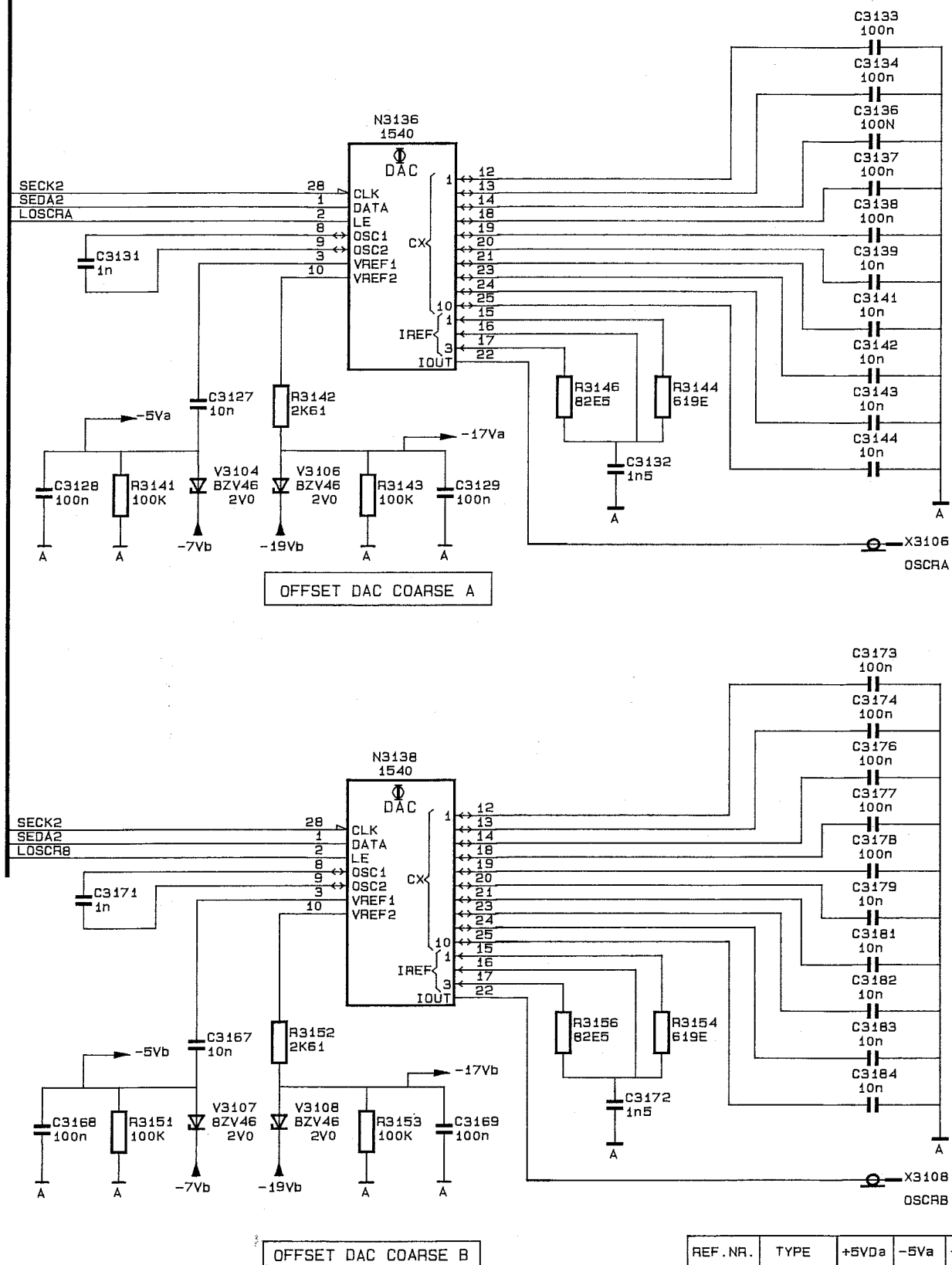


I
MAT 3251



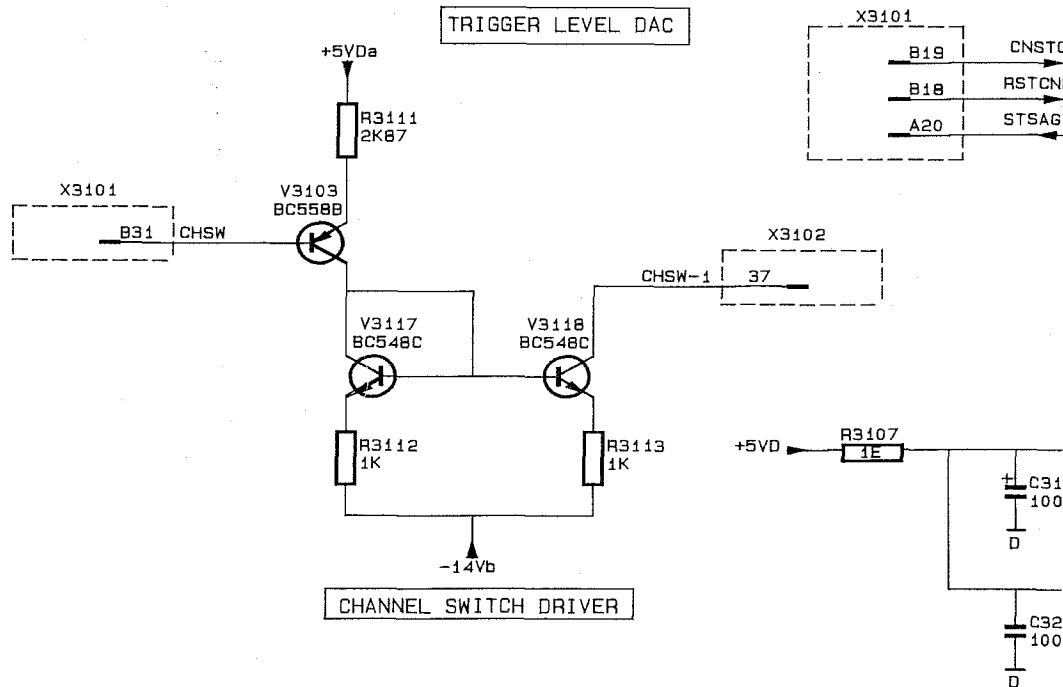
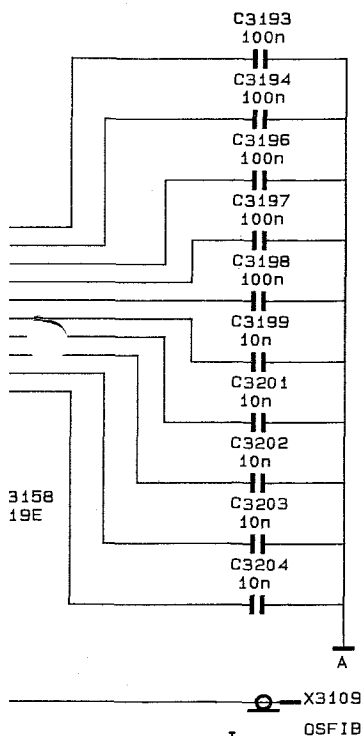
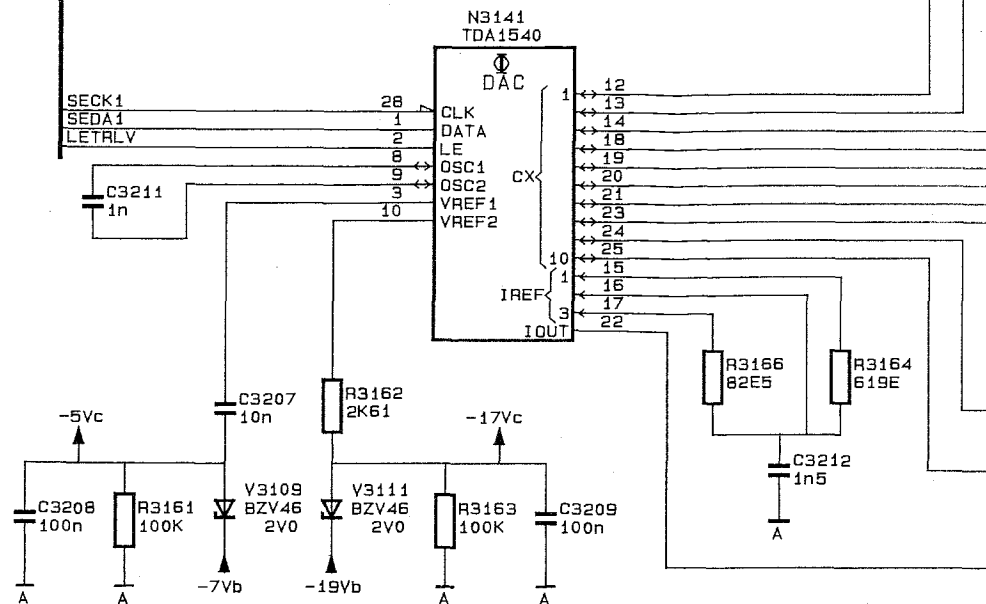
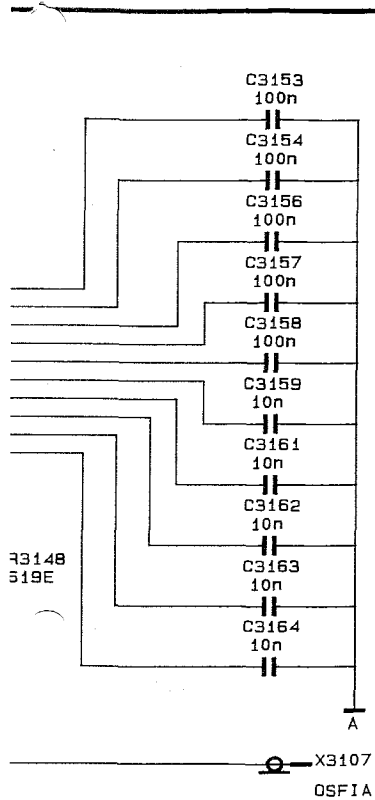
REF. NR.	TYPE	+5VDb	+5VDC	+14Vb	-14Vb	I A	I D
D3142	TEA1017		7				3
D3144	TEA1017	7					3
N3143	AD7541			16		3	
N3146	AD7541			16		3	
N3147	HA2525		7	4			
N3148	HA2525		7	4			

MAT 3251 II

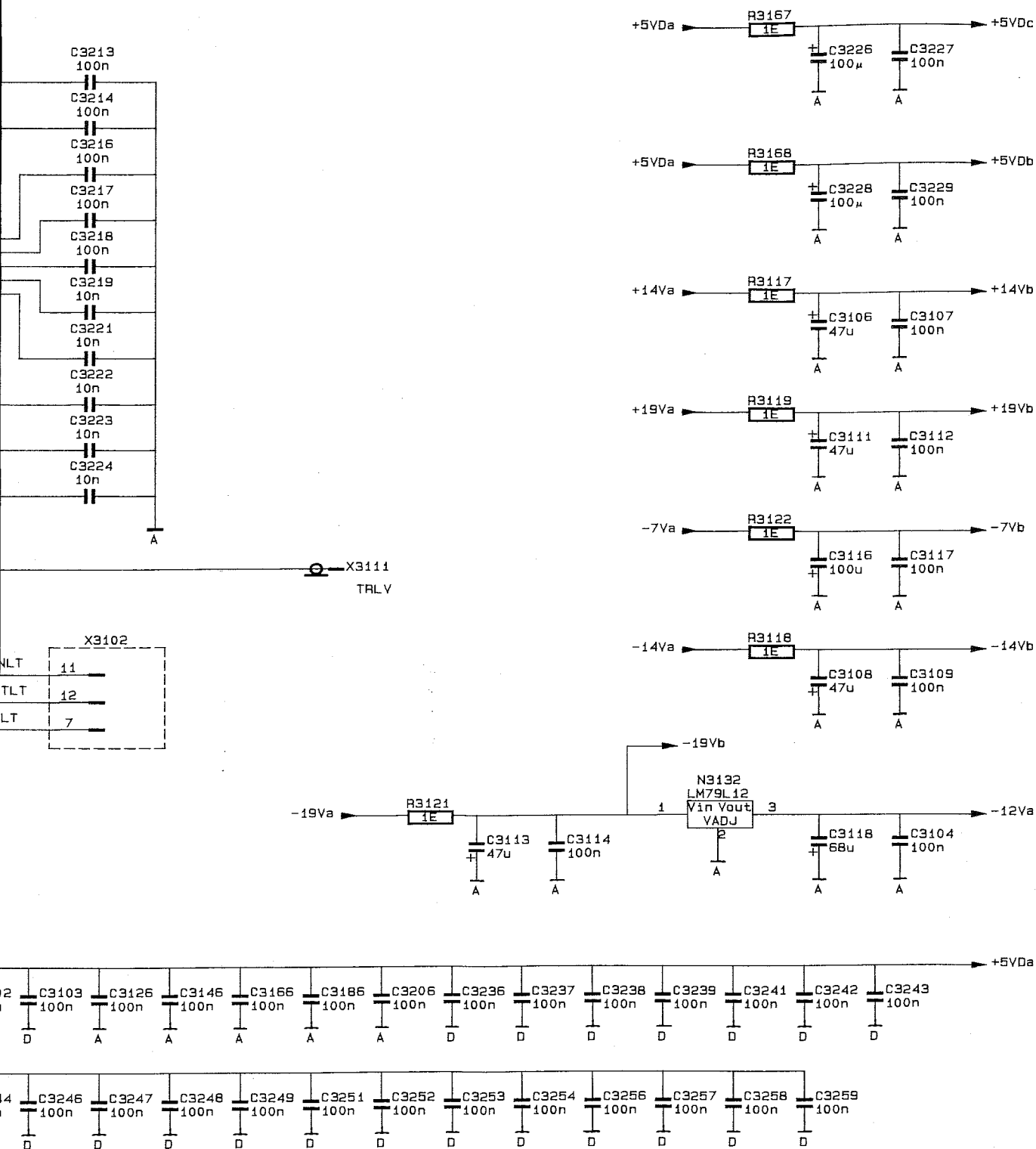


REF. NR.	TYPE	+5Vda	-5Va	-5Vb	-17Va
N3136	TDA1540	4	7		11
N3137	TDA1540	4	7		11
N3138	TDA1540	4		7	
N3139	TDA1540	4		7	

Figure 8.25.4 Unit A25 - MANAGEMENT UNIT - circuit diagram.



MAT 3252



8

MAT 3252 II

REF. NR.	TYPE	+5V _{Da}	-5V _c	-17V _c	$\frac{1}{D}$
N3141	TDA1540	4	7	11	6