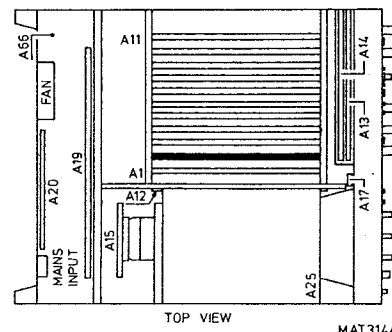


UNIT A2 - DISPLAY DAC UNITCONTENTS

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8.2.5	Signal-name list.....	8.2-11

## 8.2.1 General information

This unit basically comprises the vertical and horizontal position adders and the vertical and horizontal digital to analog converters.

## 8.2.2 Vertical data path

The vertical trace data as well as all kinds of vertical text data on the ten output lines DCDB00...DCDB09 of the display control latch is applied to a combined invert/vertical-expand/latch circuit. This circuit consists of the two (not identical) field programmable logic sequencers (FPLS) D2301 and D2302 and the D-type flip flops D2309.

The control signal IVCDB determines whether the data bits have to be inverted or not and the two control signals EPY-00 and EPY-01 determine the vertical expand factor of the circuit.

Vertical expand factor	Control signals		Digital expand factor (UNIT A2)	Analog expand factor (UNIT A1)
	EPY-01	EPY-00		
Y/5 (trace)	0	0	/4	/1,25
Y*1 (trace + MSC text)	0	1	x1	x1
line + softkey text	1	0	x4	x1
Y*5 (trace)	1	1	x4	x1,25

The combination of the digital expand factor on the display dac unit A2 and the analog expand factor on the final amplifier unit A1 results in the total required expand factor.

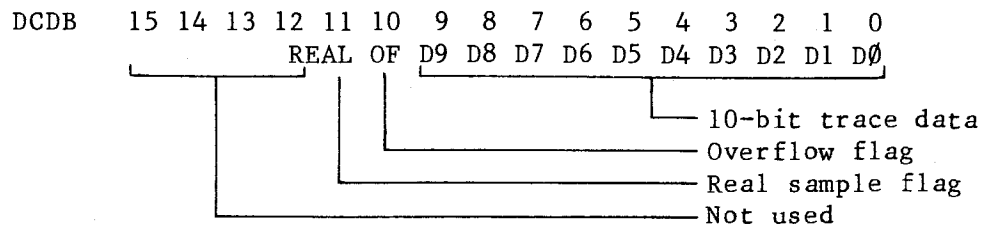
Digital expand is realized by the shifting of the bit pattern two bits to the right (/4) or two bits to the left (x4).

The resulting vertical data is then latched in the output latches of the FPLS circuits and in the four D-type flip flops by signal CKEPVE.

The data can be divided into five different kinds of data.

1) Trace data for X=t display:

Data format:



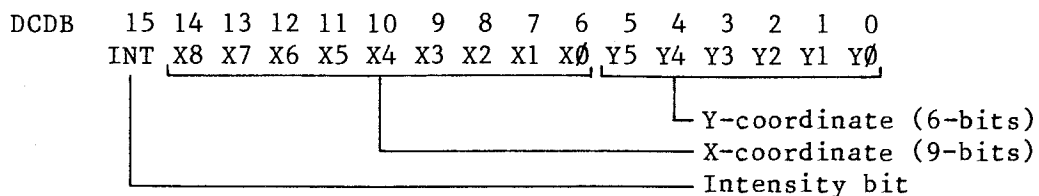
The trace data can be inverted, expanded by factors /5, x1 or x5 before it is applied as EPVE00...EPVE11 to the vertical position adder.

2) Trace data for AVSB display:

Data has the same format as for X=t display which is described before. However, only channel B is latched and applied to the vertical position adder.

- 3) Line text display:
- |                  |        |
|------------------|--------|
| Top area text    | (TAT)  |
| Trace area text  | (TRAT) |
| Bottom area text | (BAT)  |

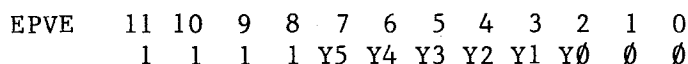
Data format:



Only 10 bits DCDB00...DCDB09 of this bit pattern are applied to the circuit and only the Y-coordinate bits Y0...Y5 are of interest.

The data is not inverted but expanded by a factor of x4 by shifting the pattern two bits to the left and switching the lowest two bits to zero. Signal ENTXLNLT is active and the output bits EPVE08...EPVE11 of D2309 are switched to one.

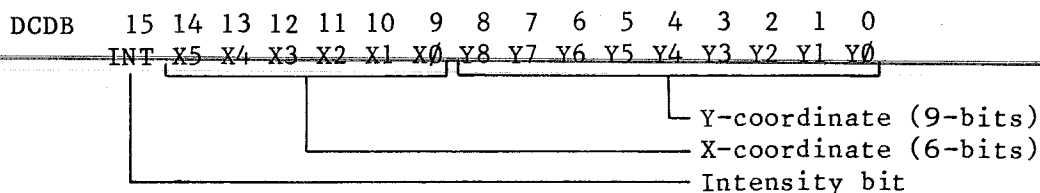
The final bit pattern is:



This pattern is applied to the vertical position adder.

4) Softkey text display (SKT):

Data format:



Only 10 bits DCDB00...DCDB09 of this bit pattern are applied to the circuit and only the nine Y-coordinate bits Y0...Y8 are of interest.

The data is not inverted but expanded by a factor of \*4 by shifting the pattern two bits to the left and switching the lowest two bits to zero.

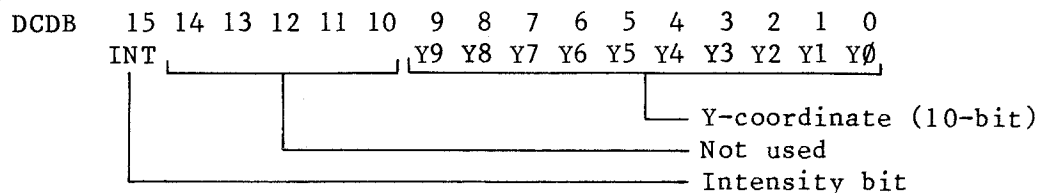
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0	
	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	0	0

This pattern is applied to the vertical position adder.

5) Miscellaneous text (MCS):

Data format Y-coordinates:



For miscellaneous text, two words, one carrying the Y-coordinate and the other one carrying the X-coordinate, are placed in the text memory for each dot to be displayed.

Only the 10 bits DCDB00...DCDB09 of the Y-coordinate pattern are applied to the circuit.

The data is not inverted and not expanded.

The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

This pattern is applied to the vertical position adder.

The output signal Z-OT01LT of the first FPLS circuit D2301 is applied to the second one and the output signal Z-OT02LT of the second FPLS circuit D2302 is applied to a reflection detection circuit.

The vertical position adder is a sixteen bit circuit which consists of D2319, D2321, D2324 and D2326. A sixteen bit vertical position information is latched in the vertical position latches D2314 and D2316 by signal WRVEPOLT and applied to the other adder input side. This vertical position information is calculated by the microprocessor ~~and depends on the selected vertical expand factor, the use of the Y-POSITION control and the type of trace or text which has to be displayed.~~

The adder output bits VEDB09...VEDB11 are carrying information about reflection and are applied to a Z-detection circuit on unit A3. The following combinations result in light on the C.R.T. screen.

VEDB	11	10	09	08
	0	0	0	1
	1	1	1	0

All other combinations result in NO light on the C.R.T. screen. This has no function for text display.

The other ten adder output bits VEDB00...VEDB09 which carry information in two-complement notation, are first converted by the code convert circuit D2338 into straight binary notation by inverting the highest bit VEDB09. These converted ten bits are then latched for a time of 750 ns (time between two dots) in a YDAC latch consisting of D2329 and D2331. This is done by the signal LEDA-1HT. It is then applied to the 10-bits vertical digital-to-analog converter YDAC N2301 which has two symmetrical output current lines. A constant reference voltage +10VREF from differential amplifier N2304 is applied to the YDAC.

The symmetrical output currents of the YDAC are converted into voltage levels by a Hooper stage with low input impedance and low output impedance. This Hooper stage is formed by the transistors V2301 and V2302. The signals are fed then to sample and hold circuits with switches D2341, capacitors C2366 and C2367 and field effect transistors V2303 and V2303 for the deglitching of the YDAC output signals. This is necessary for dot-join display because the trace is constantly unblanked then.

As long as the YDAC outputs are not stable, the switches D2341 are opened by the signal LEDA-1LT and the previous levels are held (for about 125 ns) over the capacitors C2366 and C2367 and at the inputs of the FET transistors V2303 and V2303. After 125 ns the YDAC outputs are stable and the switches are closed. The capacitors can then be charged to the new YDAC output levels. In this way, the YDAC output glitches are suppressed.

For display of only discrete dots, the S/H output signals are applied via an output buffer of two emitter followers V2304 and V2307 with high input impedance and low output impedance as Y1IN and Y2IN to the inputs of the vertical final amplifier stage on unit A1.

For dot-join display an RC-filter with an RC-time of 750 ns (1 dot cycle) can be switched in.

With signal DJAC--HT active, capacitor C2373 will be switched in via switch D2341. In this case only the real samples (512) will be connected with each other with lines between the dots.

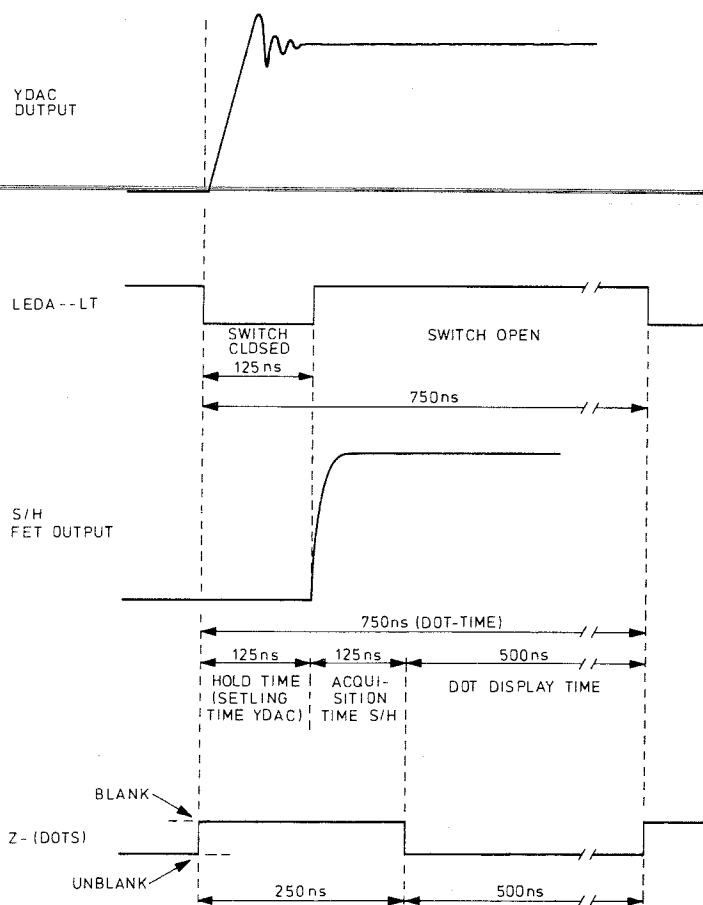
MAT2476  
861107

Fig. 8.2.1 Dot cycle

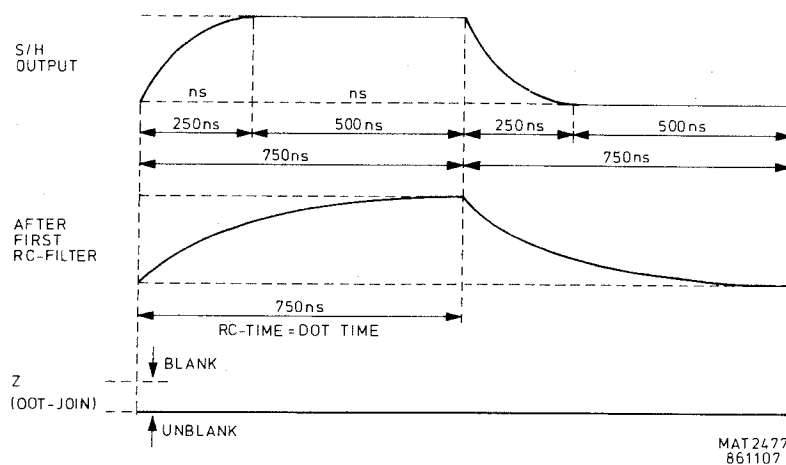
MAT2477  
861107

Fig. 8.2.2 Dot join cycle

For smooth display not only the dot-join filter is switched in, but also the smooth filter which gives a total RC-time of 7,5  $\mu$ s (10 dot cycles).

This second RC-filter is switched in when signal SM---LT is activated. Capacitor C2369 is switched in via switch D2342 and lines are displayed over ten dots.

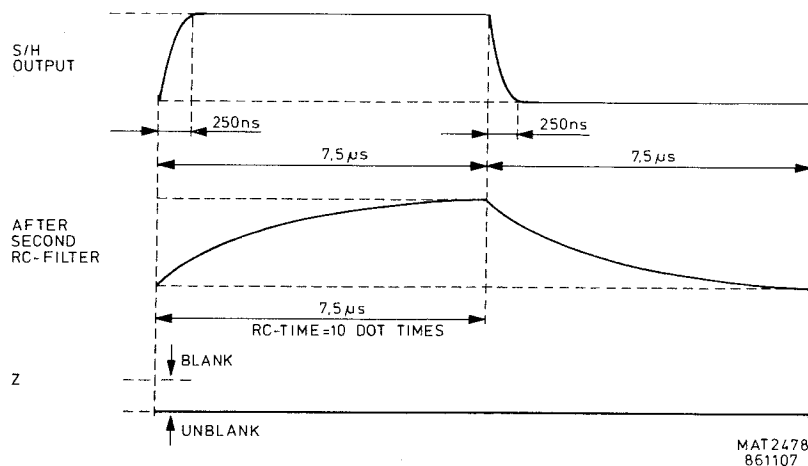


Fig. 8.2.3 Smooth cycle

NOTE: In this instrument the smooth circuit is not activated.

### 8.2.3 Horizontal data path

Horizontal data on the expand data bus lines EPDB00...EPDB111 can be divided into five kinds of data.

#### 1) Address data for X=t display:

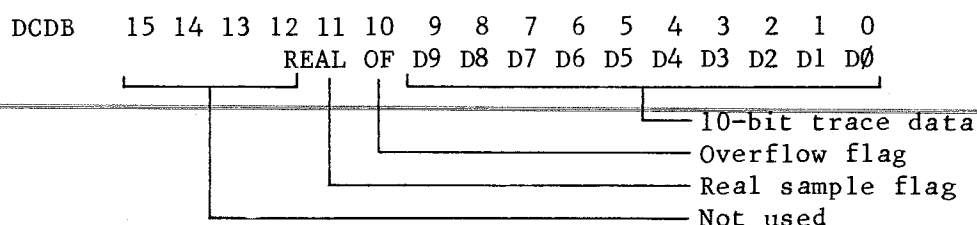
Data format:

DPAB	11	10	9	8	7	6	5	4	3	2	1	0
A	11	10	9	8	7	6	5	4	3	2	1	0

12-bit address data from the display address counter on unit A3.

The state of the display address counter is used for horizontal deflection during normal X=t display.

This data is applied to the expand data bus lines EPDB00...EPDB111 via the display address data buffer, which consists of D2121 on unit A3 and a part of D2122 on unit A3, when signal HOMO is active.

2) Trace data for AVSB display:

Vertical trace data bits DCDB00...DCDB09 of channel A for X-deflection in A versus B mode is applied to the expand data bus lines EPDB00...EPDB11 via the AVSB trace data buffer, which consists of D2303 and a part of D2304. This buffer is active when signal ENTRHOLT is activated.

The highest bit is inverted by the code convert circuit D2337 to convert the trace data from two-complement notation to straight binary notation. (For channel B this is done in the vertical channel path).

Via the AVSB trace data buffer the data is multiplied by a factor of four to adapt it to the higher horizontal resolution.

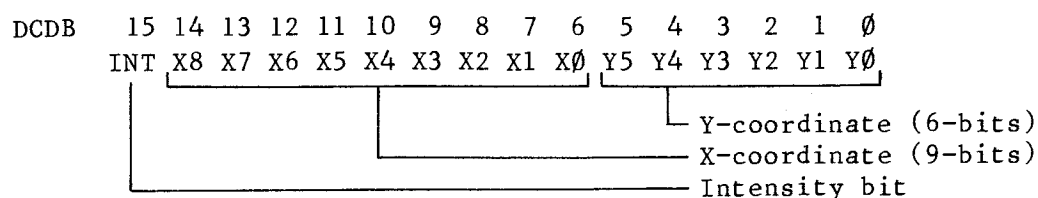
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0

This pattern is applied to the horizontal expand I circuit.

3) Line text display:      Top area text      (TAT)  
                                  Trace area text    (TRAT)  
                                  Bottom area text (BAT)

Data format:



Only the 9 X-coordinate bits DCDB06...DCDB14 or X0...X8 are of interest. These bits are applied to the expand data bus lines via the line text data buffer which consists of a part of D2304 on unit A2 and D2124 on unit A3. This buffer is active when signal ENTXLNLT is active. The data is via this line text data buffer expanded to twelve bits of which the lowest three bits are made zero.

The final bit pattern is:

EPDB	11	10	9	8	7	6	5	4	3	2	1	0
	X8	X7	X6	X5	X4	X3	X2	X1	X0	0	0	0

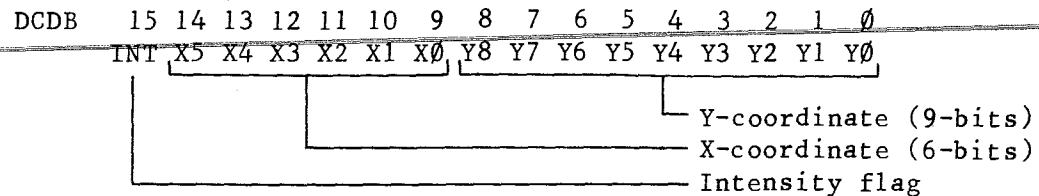
This pattern is applied to the horizontal expand I circuit.

In line text display mode, the X-variable is automatically set by the microprocessor to \*1,5.

This results in 512 horizontal text dot positions over 15 divisions, so with a dot distance of 0,293 mm.

4) Softkey text display (SKT):

Data format:



Only the six X-coordinate bits DCDB09...DCDB14 or X0...X5 are of interest. These bits are applied to the expand data bus lines via the softkey text data buffer which consists of D2133 on unit A3 and a part of D2122 on unit A3. This buffer is active when signal ENTXSKLT is active. The data is converted to twelve bits via this buffer. The highest three as well as the lowest three bits are made zero.

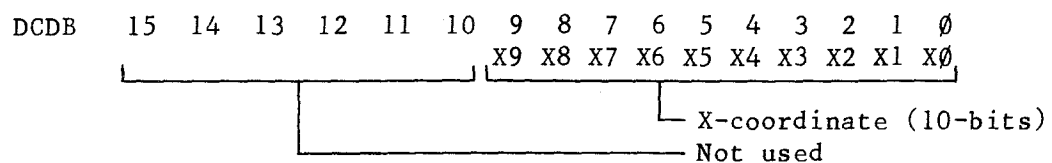
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	X5	X4	X3	X2	X1	X0	0	0	0

In softkey text display-mode the X-variable is automatically set to \*1,5 by the microprocessor. This results in 512 horizontal text dot positions over 15 divisions, so with a dot distance of 0,293 mm.

5) Miscellaneous text (MSC):

Data format X-coordinates:



For miscellaneous text, two words, one carrying the Y-coordinate and the other one carrying the X-coordinate, are placed in the text memory for each dot to be displayed.

Only the 10 bits DCDB00...DCDB09 of the X-coordinate pattern are applied to the circuit. The data is not expanded and the X-variable is set to \*1.

The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	0	0

The pattern is applied to the horizontal expand I circuit.

The expand databus is connected to the horizontal expand I circuit consisting of a number of multiplexers. The first group D2305, D2307 and D2308 is able to shift the input bit pattern one bit to the left or not. This means that an expand factor \*1 is selected if signal EXP-00 is "0" and that an expand factor of \*2 is selected if signal EXP-00 is "1". The second group D2311, D2312 and D2313 is able to shift its input bit pattern two bits to the left or not.

This means that an expand factor \*1 is selected if signal EXP-01 is "0" and that an expand factor of \*4 is selected if signal EXP-01 is "1".

The combination of these two groups results in a circuit of which the expand factor can be switched to \*1, \*2, \*4 or \*8 depending on the signals EXP-00 and EXP-01.

The twelve lines EPH000...EPH011 of the expand horizontal data bus are applied to one input side of a sixteen bit horizontal adder circuit which consists of D2322, D2323, D2327 and D2328.

A sixteen bit horizontal position information is latched in the horizontal position latches D2317 and D2318 by signal WRHOPOLT and applied to the other adder input side.

This horizontal position information is calculated by the microprocessor and depends on the selected horizontal expand factor, the use of the X-POSITION control and the type of trace or text which has to be displayed.

The signals HODB13, HODB14 and HODB15 are applied to a reflection detection circuit.

The adder output bits HODB00...HODB12 are applied to a horizontal expand II circuit which consists of the multiplexers D2333, D2334 and D2336. This circuit can be switched for an expand factor \*1, when signal EPX-02 is "0" and to a factor \*8, when signal EPX-02 is "1".

- \*1 The address range is shifted three bits to the left resulting in 512 horizontal display positions over ten divisions
- \*8 Only the lowest 10 bits of the address range is used resulting in an horizontal expand factor of \*8.

Data is latched in the multiplexers by signal LEDA--LT and DPRJ.

Ten bits of the horizontal expand II circuit output data are applied to the 10-bits horizontal digital to analog converter XDAC (N2303) which has two symmetrical output current lines. A constant reference voltage +10VREF from differential amplifier N2304 is applied to the XDAC. The symmetrical output currents of the XDAC are furthermore handled like already described under 8.2.2. for the vertical data path. Afterwards they are applied as X1IN and X2IN to the inputs of the horizontal final amplifier stage on unit A1.

## 8. 2.4 X-variable data path

X-variable data which depends on the use of the X-EXPAND rotary controls, is calculated by the microprocessor and placed on the data bus lines DB08...DB15. It is then latched in the X-variable latch

D2332 when signal WRHOVRLT is active.

It is then applied to an 8-bit X-variable digital to analog converter N2302. A constant reference voltage +10VREF from differential amplifier N2304 is applied to the DAC. The symmetrical output current lines VREPX1 and VREPX2 are applied to the horizontal final amplifier stage on unit A1.

## 8. 2.5 Signal-name list

## UNIT A2

Signal-name	Description	Signal source	Signal destination(s)
CKEPVE	Clock expand vertical	A3	-
DB00...15	Data bus 00...15	A6+option	-
DCDB00...09	Display control data bus 00...09	A4	-
DIOS--HT	Disable overscan	A3	-
DJAC--HT	Dot join active	A3	-
DPRJUP	Display reject up	A3	-
DPRJDW	Display reject down	A3	-
DPRJDW01	Display reject down	A2	A2
ENTRHOLT	Enable trace horizontal	A3	-
ENTXLNLT	Enable text line	A3	-
EPDB00...11	Expanded data bus 00...11	A2, A3	A2
EPHO00...13	Expanded horizontal bus 00...13	A2	A2
EPHO14	Expanded horizontal bus 14	A3	-
EPVE00...11	Expanded vertical bus 00...11	A2	A2
EPVE08LT	Expanded vertical bus 08	A2	A2
EPVE09LT	Expanded vertical bus 09	A2	A2
EPX-00...02	Expand X 00...02	A3	-
EPY-00...01	Expand Y 00...01	A3	-
EP12--LT	Expand 12	A3	-
IVDCDB	Invert display control address bus	A3	-
LEDA--LT	Latch enable DAC	A3	-
LEDA-1LT	Latch enable DAC	A2	A2
LEDA--HT	Latch enable DAC	A3	-
LEDA-1HT	Latch enable DAC	A2	A2
HODB00...15	Horizontal data bus 00...15	A2	A2
HOP000...15	Horizontal position bus 00...15	A2	A2
SM---LT	Smooth	A3	-

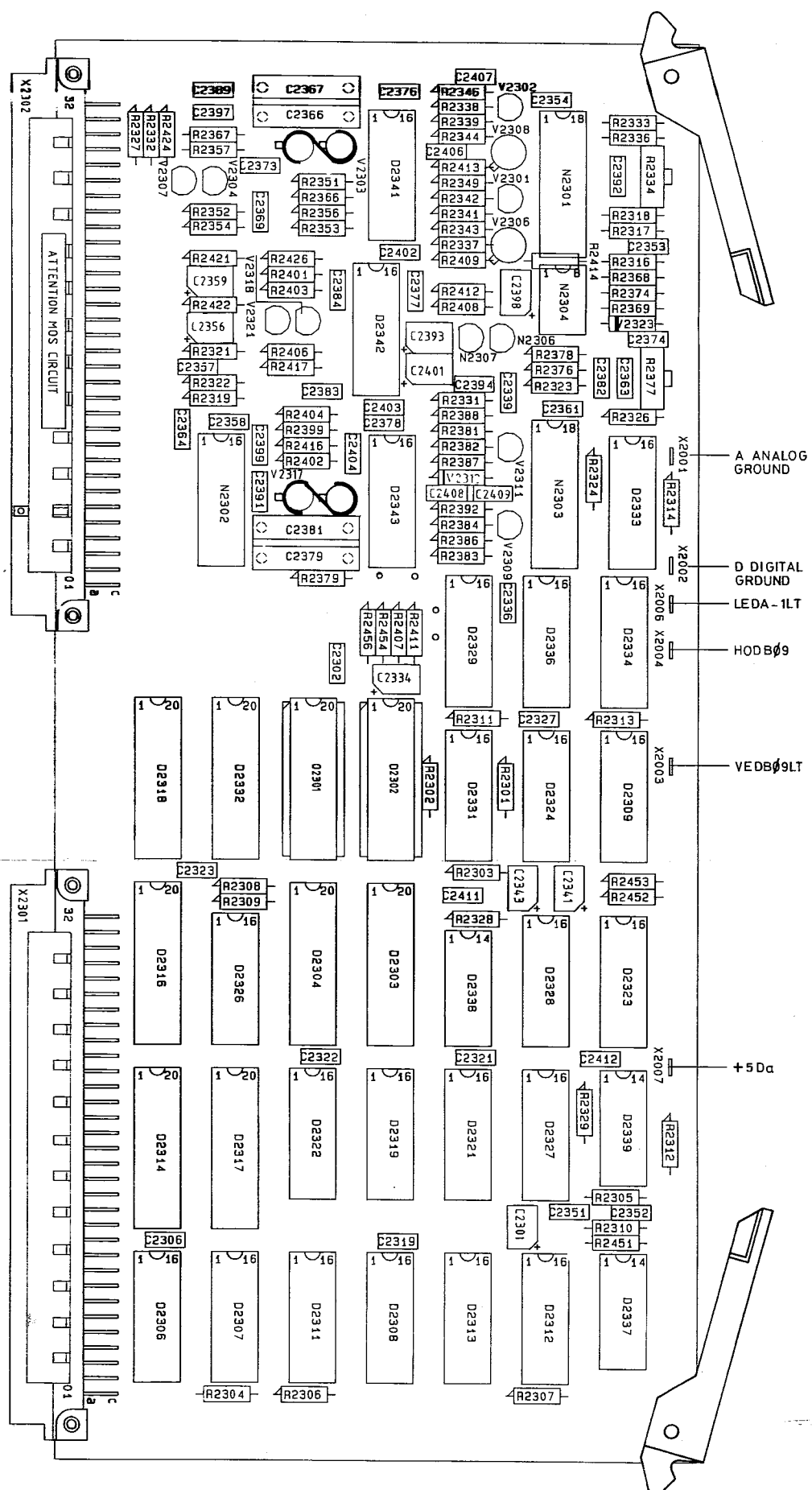
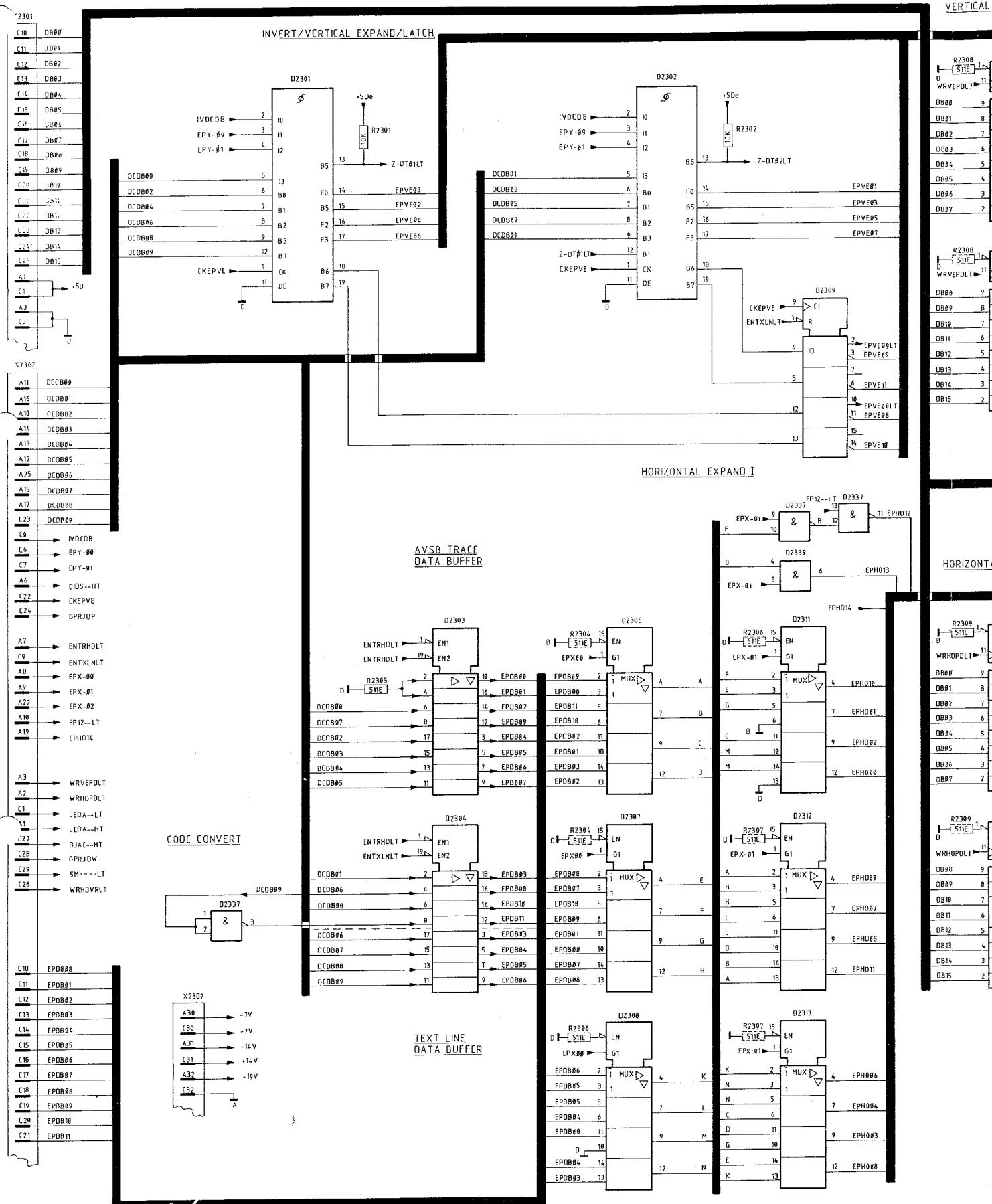


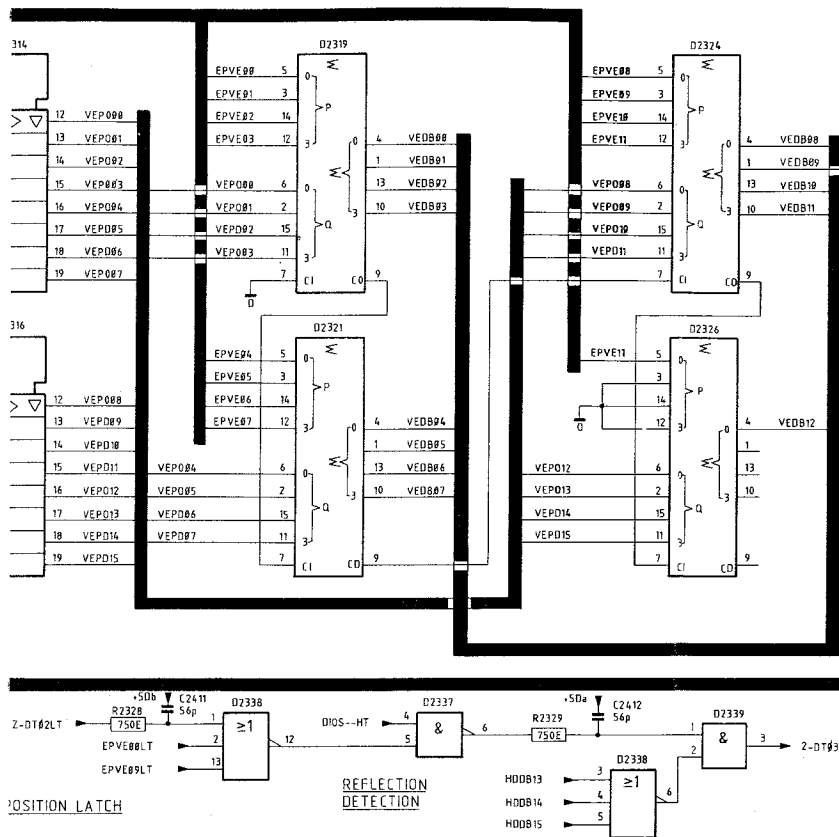
Figure 8.2.4 Unit A2 - DISPLAY DAC UNIT - p.c.b. lay-out.

MAT2532A  
880205

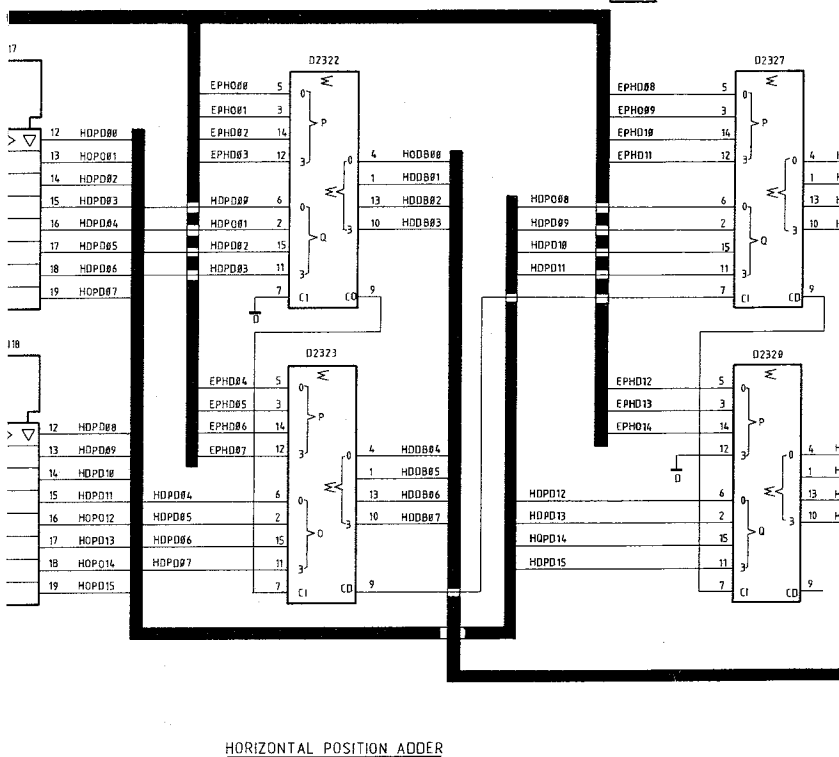


# SITION LATCH

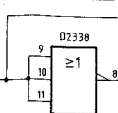
# VERTICAL POSITION ADDER



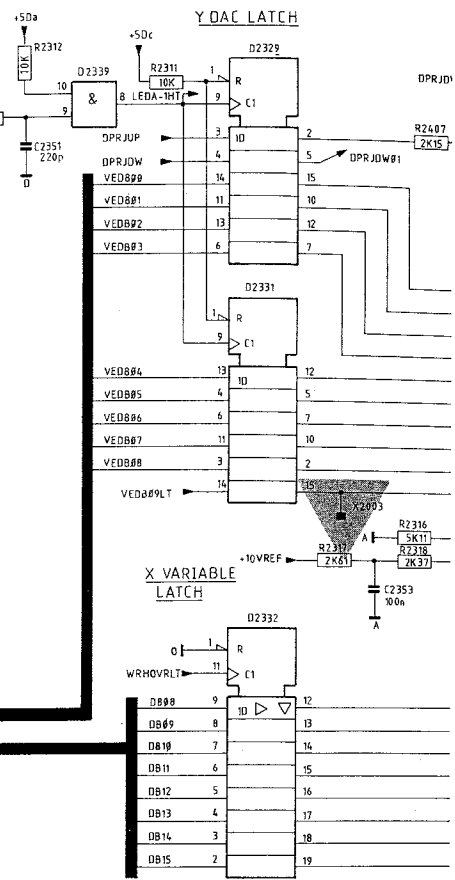
# POSITION LATCH



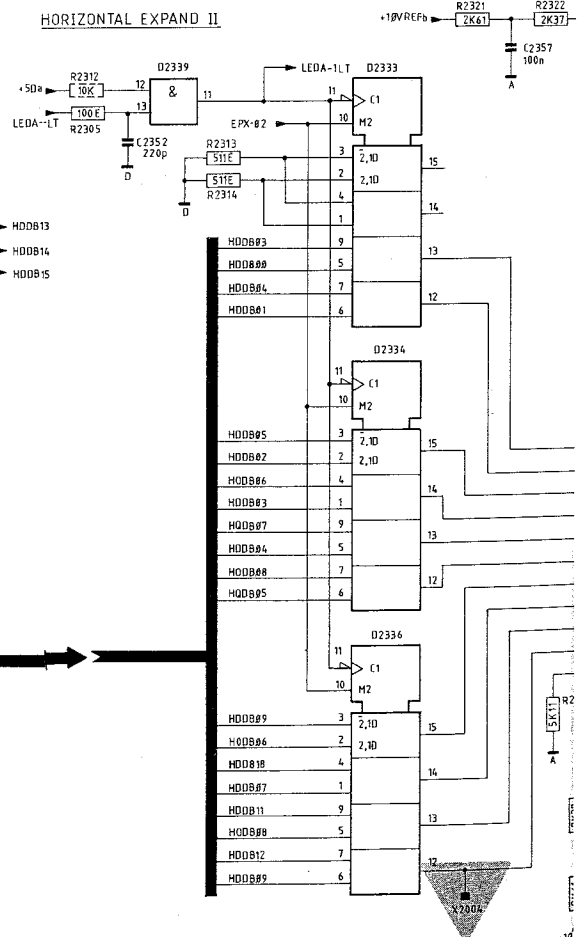
# CODE CONVERT



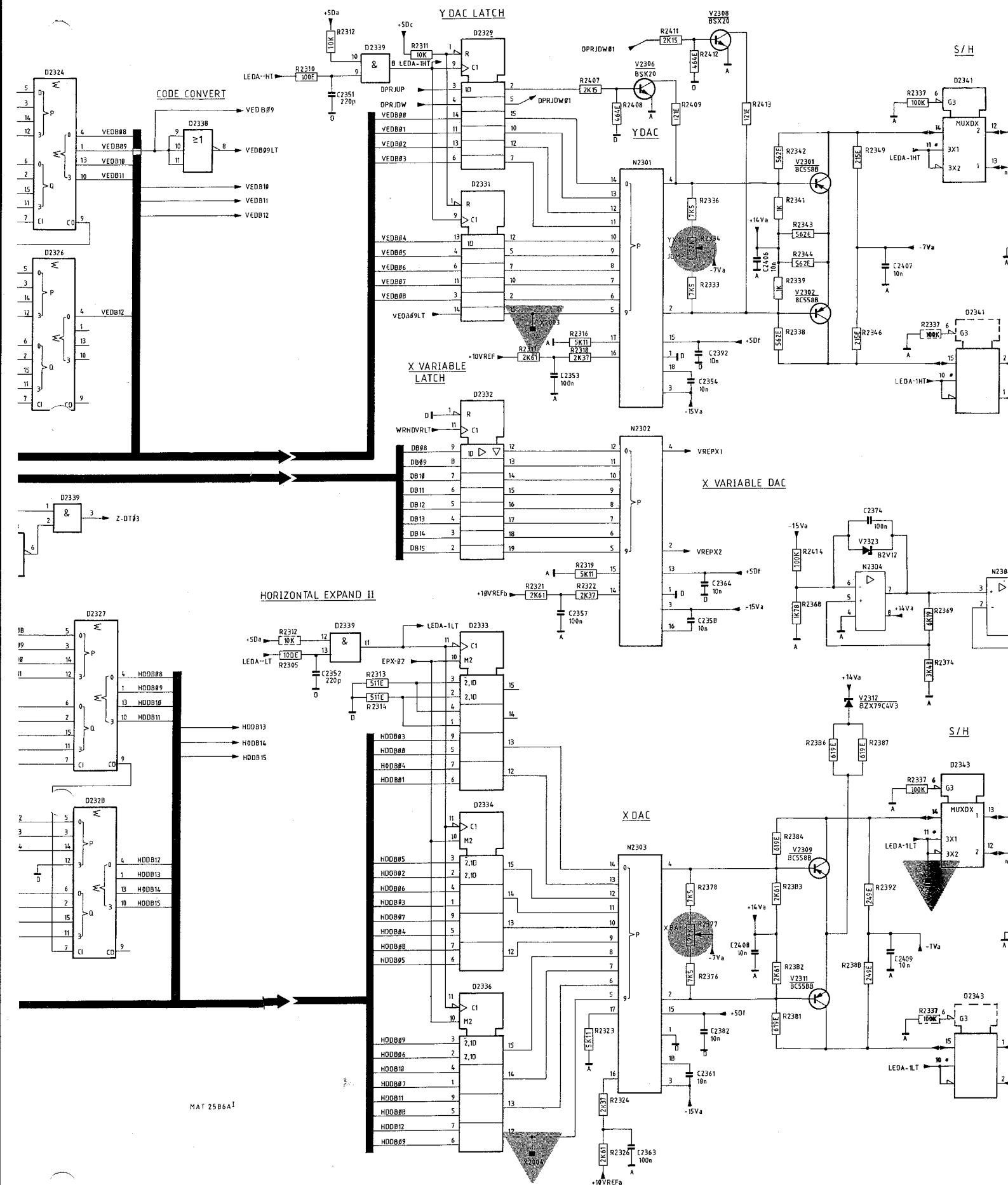
# Y OAC LATCH

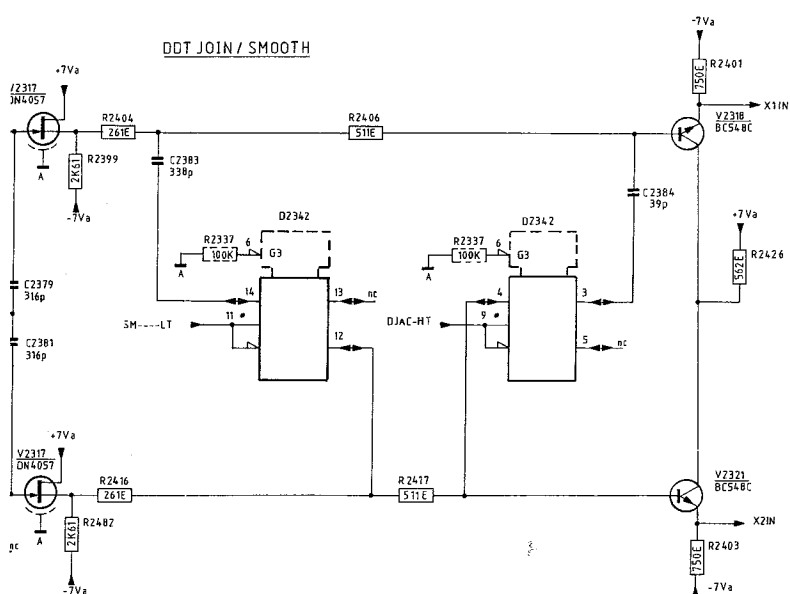
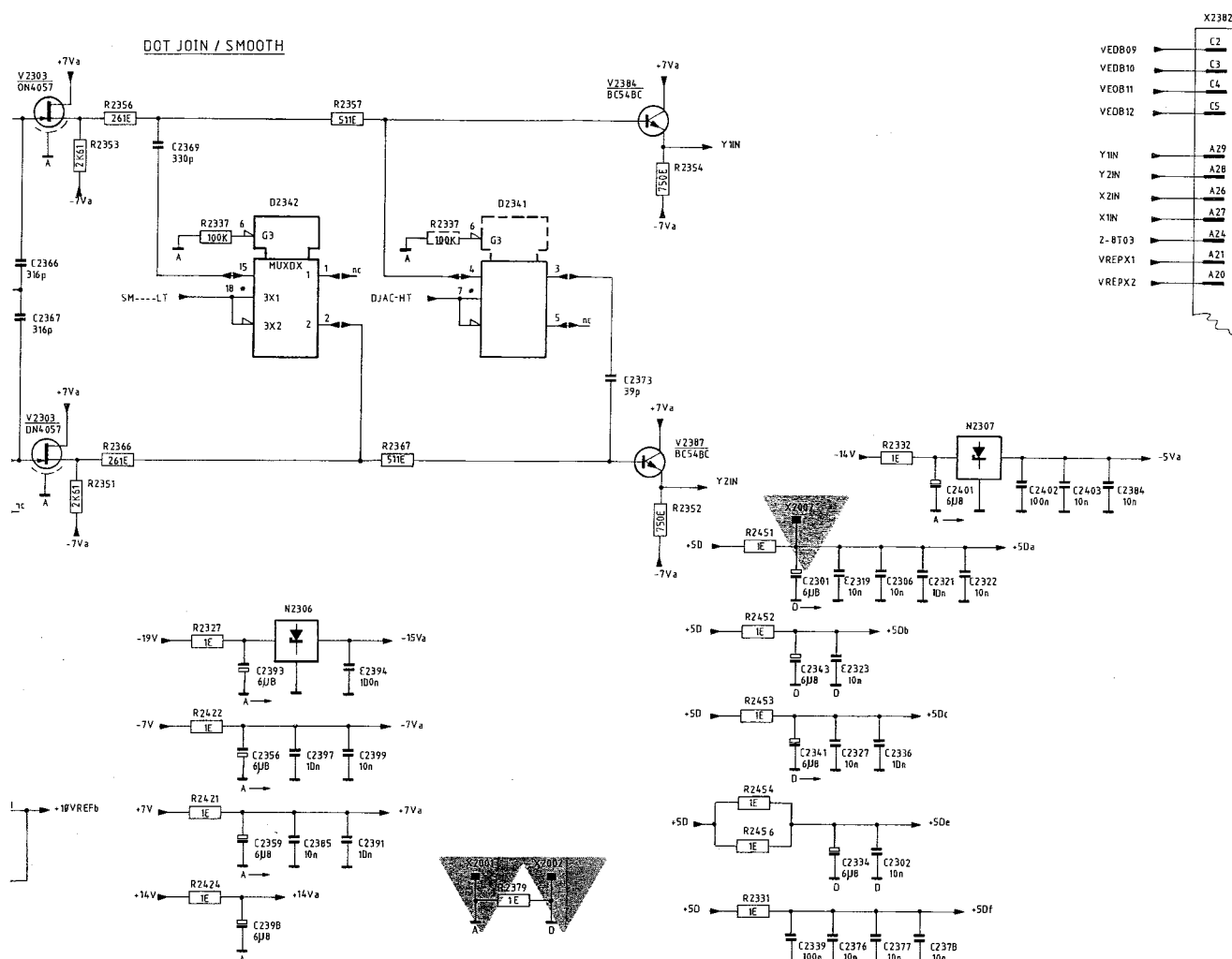


# HORIZONTAL EXPAND II



MAT 2586A1





		Vcc AND GND PIN CONNECTIONS							
REF. NR.	TYPE	-50a	-50b	-50c	-50d	-50e	-50f	-50g	-50h
D2381,2382	74LS165				20		10		
D2386,2387,2388	74HCT257	16					8		
D2311,2312,2313	74HCT257	16					8		
D2314,2317	74HCT574	28					10		
D2316,2318,2332	74HCT574						10		
D2319,2321,2322	74LS283	16	20				8		
D2323,2326,2328	74LS283	16					8		
D2324	74LS283		16				8		
D2327	74LS283	16					8		
D2389	74HCT175		16				8		
D2329,2331	74HCT174		16				8		
D2333,2334,2336	74LS298		16				8		
D2341,2342	74HCT4053			16			8	7	
D2343	74HCT4053			16			8	7	
D2337	74HCT00	14					7		
D2338	74HCT27	14					7		
D2339	74HCT08	14					7		
N2301,2303	DAC08P			15			1		3
N2302	DAC08P			13			4		8
N2304	LM358P								
N2306	LH79L15								
N2307	LH79L05								
D2303,2304	74HCT244	20					10		