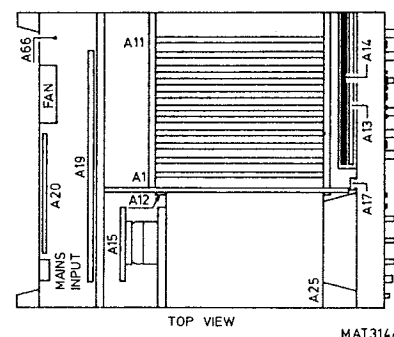


UNIT A14 - FRONT 2CONTENTS

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8.14.1 General information

This front unit contains all the front-panel optical switches and their photo-sensitive transistors.
There are eleven identical optical switches for the following functions:

X-POSITION
X-EXPAND
VARIABLE-B
Y-POSITION
OFFSET-A
VARIABLE-A
OFFSET-B
1st CURSOR
2nd CURSOR
LEVEL
HOLD OFF/SYNC

8.14.2 Optical switches

The rotation of an optical switch is detected by the two internal photo-transistors. If the control is turned from one position to another, light from the infra-red LED's falls in the photo-transistors, pulsed via the holes in a perforated disc. As a result, the photo-transistors conduct for some time and their collectors are low.

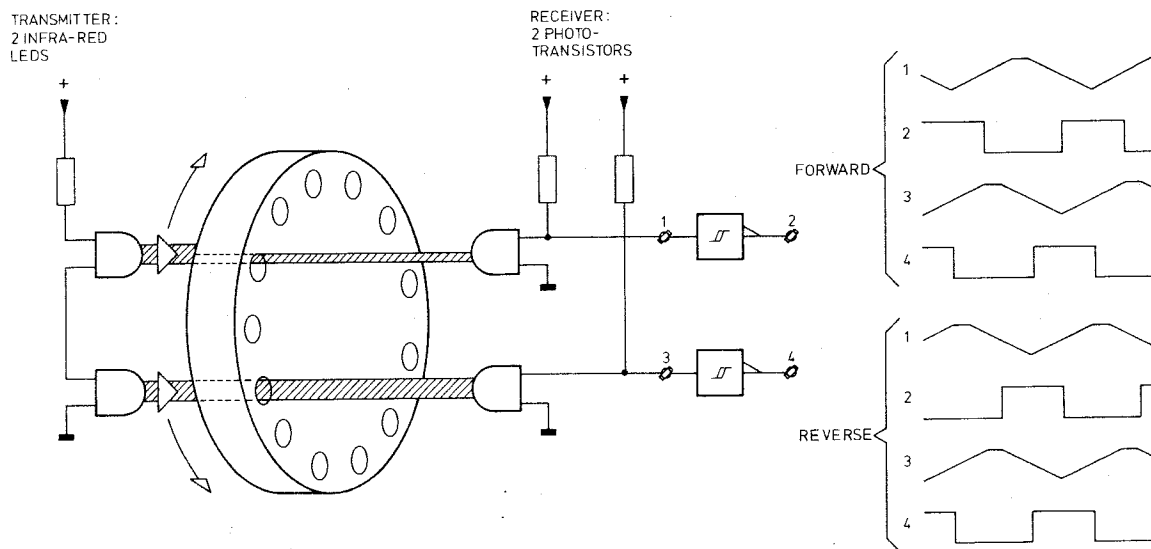


Figure 8.14.1 Optical switches

MAT 2481

The collector signals of the photo-transistors are applied to three 3-state registers D4012, D4011, and D4009 as rotate forward signals RTFW01 ... RTFW12 and rotate backward signals RTBW01 ... RTBW12. This is done via SCHMITT-trigger inverters for good pulse definition.

If one of the optical switches is operated, the relevant RTFW.. pulse is used for the generation of an interrupt level pulse IL03PU on output point 9 of NAND D4014 on each positive or negative going signal edge.

This pulse is used as clockpulse for the D-type flip flop D4016, resulting in an interrupt level signal IL03--LT which interrupts the microprocessor. This is done to realize a very quick reaction by the microprocessor when an optical switch is operated.

The flip flop output signal IL03--HT is used to clock the actual photo-transistor output levels in the three 3-state registers via the databus lines DB00 ... DB07 for further processing.

In this way the microprocessor knows which switch is operated and in which direction.

The microprocessor will be interrupted by signal IL03--LT and generates in turn three different addresses and the UPRD--LT signals in order to read the contents of the 3-state registers.

If a front unit address is generated, the IO select signal IOSL04LT for the front unit will be active.

Selection of one of the 3-state registers is achieved then by decoder D4013, which decodes the three microprocessor address lines AB01, AB02 and AB03. This results then in one active low decoder output line (enable rotate) ENRT01, ENRT02 or ENRT03. This are the output enable signals for the three 3-state registers and the one which is enabled places its data on the microprocessor data bus lines DB00... DB07.

During the read cycle, flip flop D4016 will be set to its zero state again by signal ENRT01.

8.14.3 Address decoding table

The addresses which are generated by the microprocessor are decoded by address decoder D4013 according to the following table.

| IOSL04LT | AB04 | AB03 | AB02 | AB01 | Function |
|----------|------|------|------|------|----------|
| 0 | 1 | 0 | 0 | 0 | ENRT01 |
| 0 | 1 | 0 | 0 | 1 | ENRT02 |
| 0 | 1 | 0 | 1 | 0 | ENRT03 |

8.14.4 Signal name list

UNIT A14

| Signal name | Description | Signal source | Signal destination(s) |
|-------------|-------------------------|---------------|-----------------------|
| AB01...04 | Address bus 01...04 | A6+option | - |
| DB00...07 | Data bus 00...07 | A6+option | - |
| ENRT01 | Enable rotate 01 | A14 | - |
| ENRT02 | Enable rotate 02 | A14 | - |
| ENRT03 | Enable rotate 03 | A14 | - |
| IL03--LT | Interrupt level 03 | A14 | A6 |
| IL03--HT | Interrupt level 03 | A14 | - |
| IL03PU | Interrupt pulse | A14 | - |
| IOSL04LT | I/O select 04 | A6 | - |
| RTBW01...12 | Rotate backward 01...12 | A14 | - |
| RTFW01...12 | Rotate forward 01...12 | A14 | - |
| UPRD--LT | Microprocessor read | A6 | - |
| UPWR--LT | Microprocessor write | A6 | - |

TO X4201
FRONT 1
UNIT A13

MAT2542
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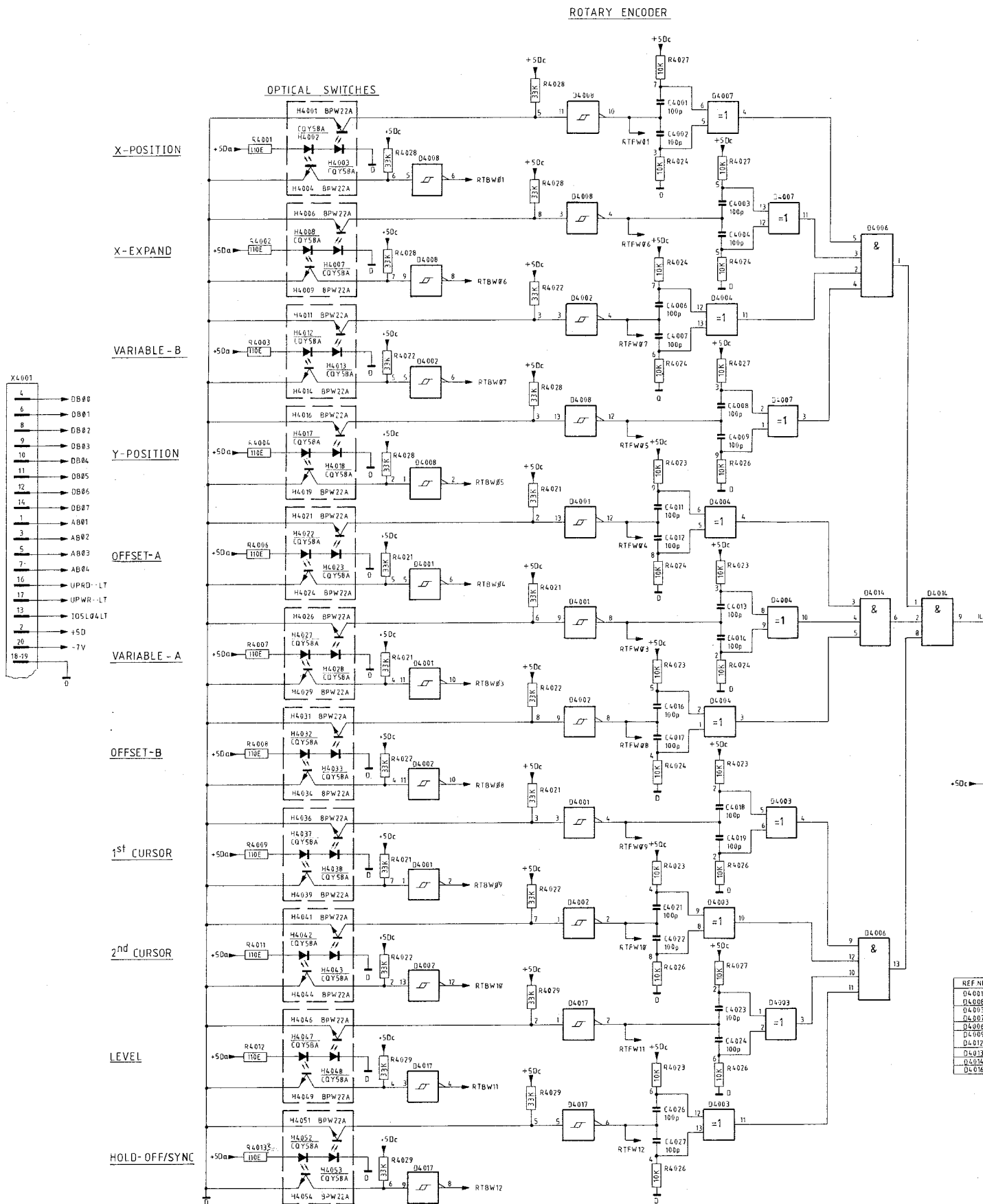
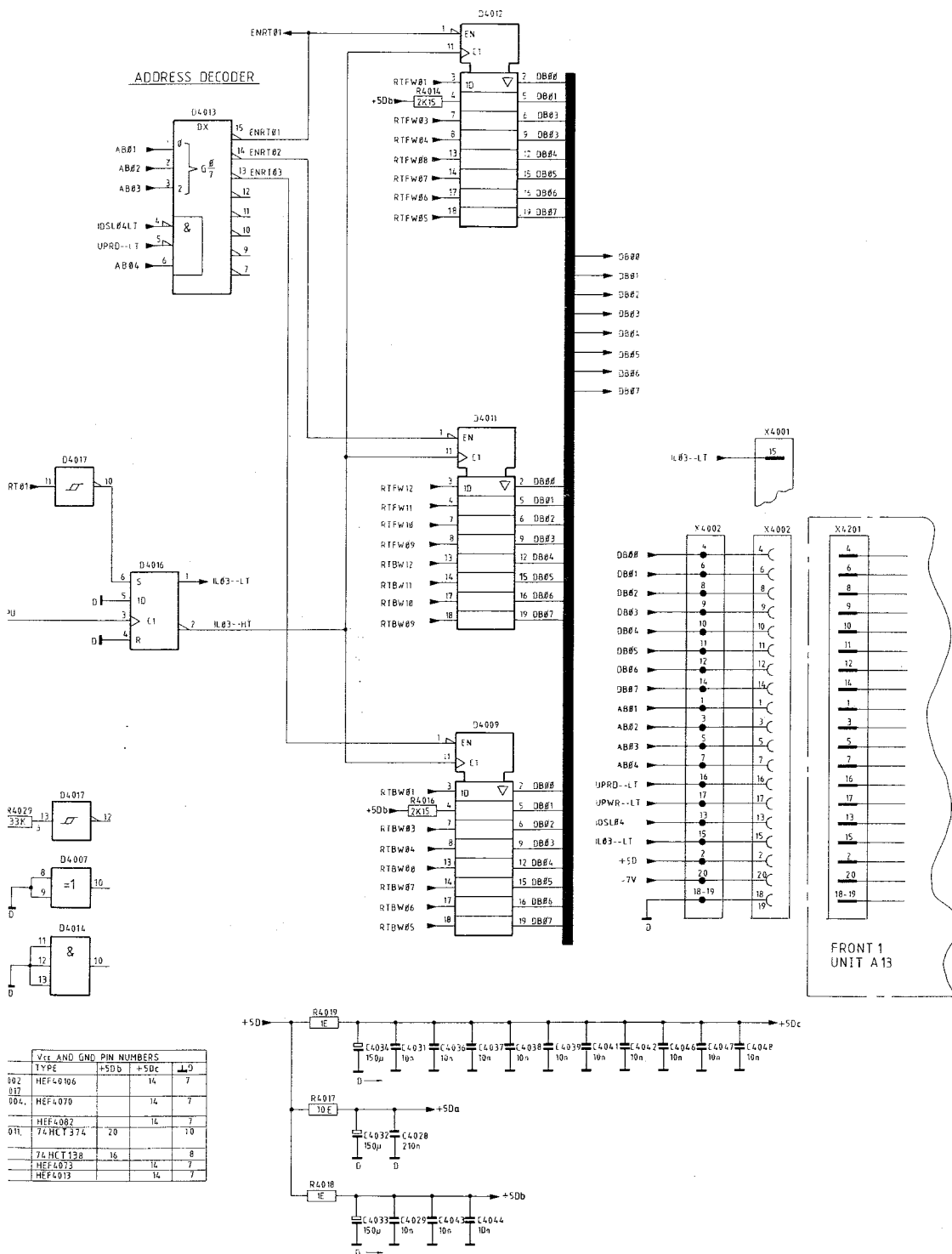


Figure 8.14.3 Unit A14 - FRONT 2 - circuit diagram.

3 - STATE REGISTER

ADDRESS DECODER

FRONT 1
UNIT A13

| Vcc AND GND PIN NUMBERS | | | |
|-------------------------|----------|------|------|
| TYPE | +5D | +5Dc | +5Da |
| 002 | HEF40106 | 14 | 7 |
| 004 | HEF40107 | 14 | 7 |
| 011 | 74HCT374 | 20 | 10 |
| | 74HCT138 | 16 | 8 |
| | HEF4013 | 14 | 7 |
| | HEF4013 | 14 | 7 |

MAT 3247