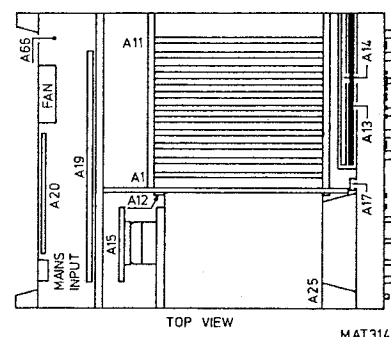


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8.13.1 General information

This front unit contains the front-panel pilot lamps, front-switches and front-switches with built-in pilot lamps.

8.13.2 Pilot lamps

The front panel pilot lamps are controlled by the microprocessor via the data bus lines DB00 ... DB07 and latches D4206 and D4207. Each latch can be activated by an output signal from the decoder D4204. This decoder decodes the three microprocessor address bits AB01, AB02 and AB03 and is enabled by the signals AB04, UPWR--LT and IOSL04LT.

This is done when the microprocessor generates the front unit addresses and the UPWR--LT signals for the control of the pilot lamps. Latch D4206 controls the pilot lamps DOTS, AVERAGE C=4, NEGATIVE SLOPE, TRIGGER, SYNCHRONIZE and COUNT DOWN.

Latch D4207 controls the pilot lamps UNCAL A, UNCAL B, REMOTE, X-EXPAND UNCAL, LOCK and WRITE.

8.13-2

8.13.3 Front-switches

The settings of all the front-switches are periodically read by the microprocessor system.

The front-switches are therefore placed in a matrix structure.

Eight switches at a time can offer their settings to the inputs of data buffer D4203.

Each row of eight switches can be activated by one of the output signals CN00 ... CN06 from the address decoder D4201. These signals are on a -0,7 V level because of the -0,7 V level on input 3 of D4201. In this way the 0,7 V across the diodes is compensated and the signals RW00 ... RW07 are brought on a 0 V level.

This decoder decodes the three microprocessor address bits AB01, AB02 and AB03 and is enabled by the signal combination AB04, UPRD--LT and IOSL04LT.

This combination resulting in signal ENFTSWLT is generated when the microprocessor generates the front unit addresses and the UPRD--LT signals for the reading of the soft-switch settings.

When signal ENFTSWLT is active, front switch buffer D4203 will place the matrix data RW00 ... RW07 on the data bus lines DB00 ... DB07.

The matrix is scanned by the microprocessor, every 40ms.

8.13.4 Address decoding table

The addresses which are generated by the microprocessor are decoded by address decoders D4204 and D4201 according to the following table.

IOSL04LT	AB04	AB03	AB02	AB01	Function	
					WR	RD
0	0	0	0	0	Leds (4206)	CN00
0	0	0	0	1	Leds (4207)	CN01
0	0	0	1	0		CN02
0	0	0	1	1		CN03
0	0	1	0	0		CN04
0	0	1	0	1		CN05
0	0	1	1	0		CN06

8.13.5 Signal name list

UNIT A13

Signal name	Description	Signal source	Signal destination(s)
AB01...04	Address bus	A6+Option	-
CN00...06	Count 00...06	A13	A13
COMMON1	Common line 1	A13	A18
COMMON2	Common line 2	A13	A17
DB00...07	Data bus 00...07	A6+Option	-
ENFTSWLT	Enter front switch	A13	A13
IOSL04LT	I/O select 04	A6	-
RW0...07	Row 00...07	A13	A13
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-

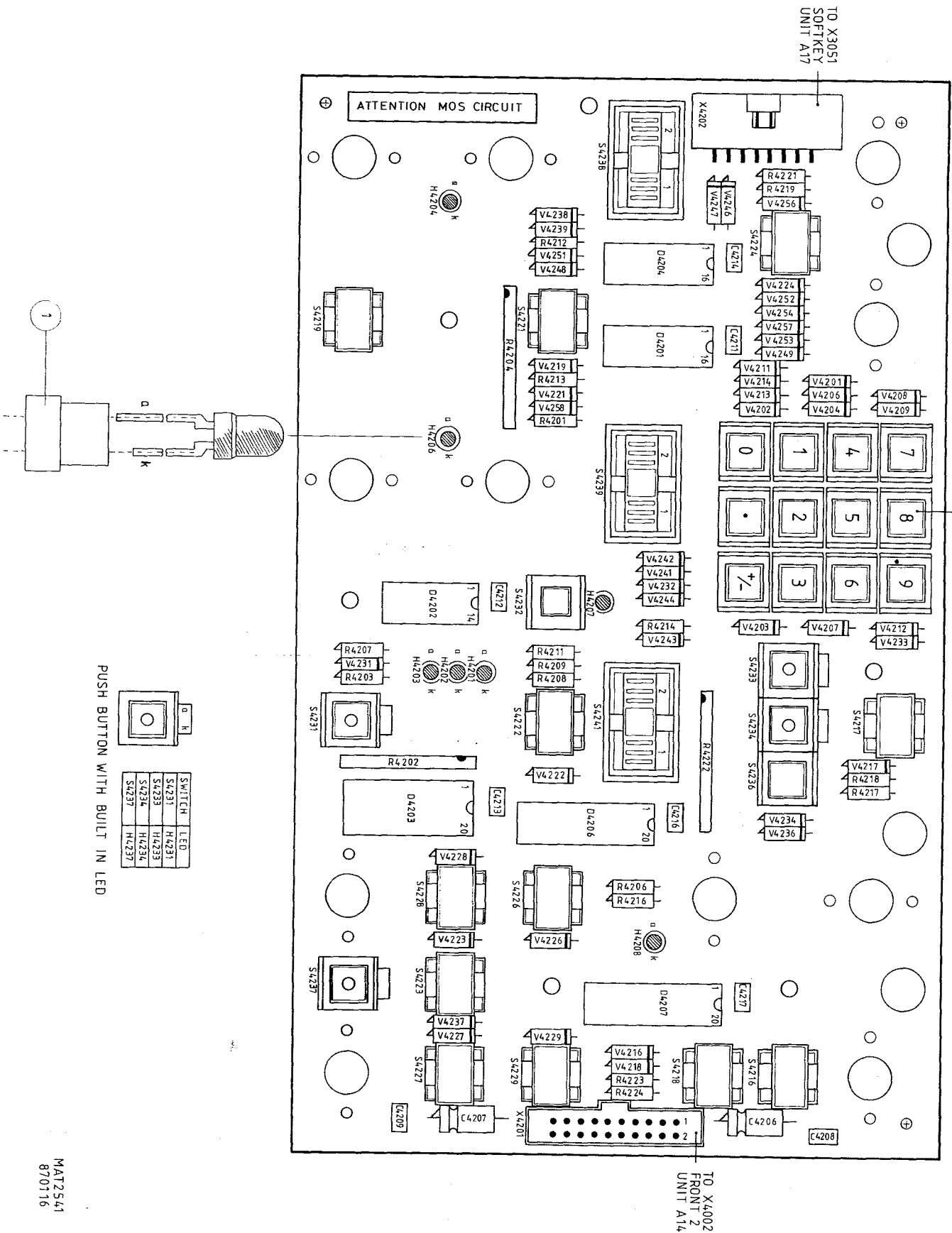


Figure 8.13.1 Unit A13 - FRONT 1 - p.c.b. layout.

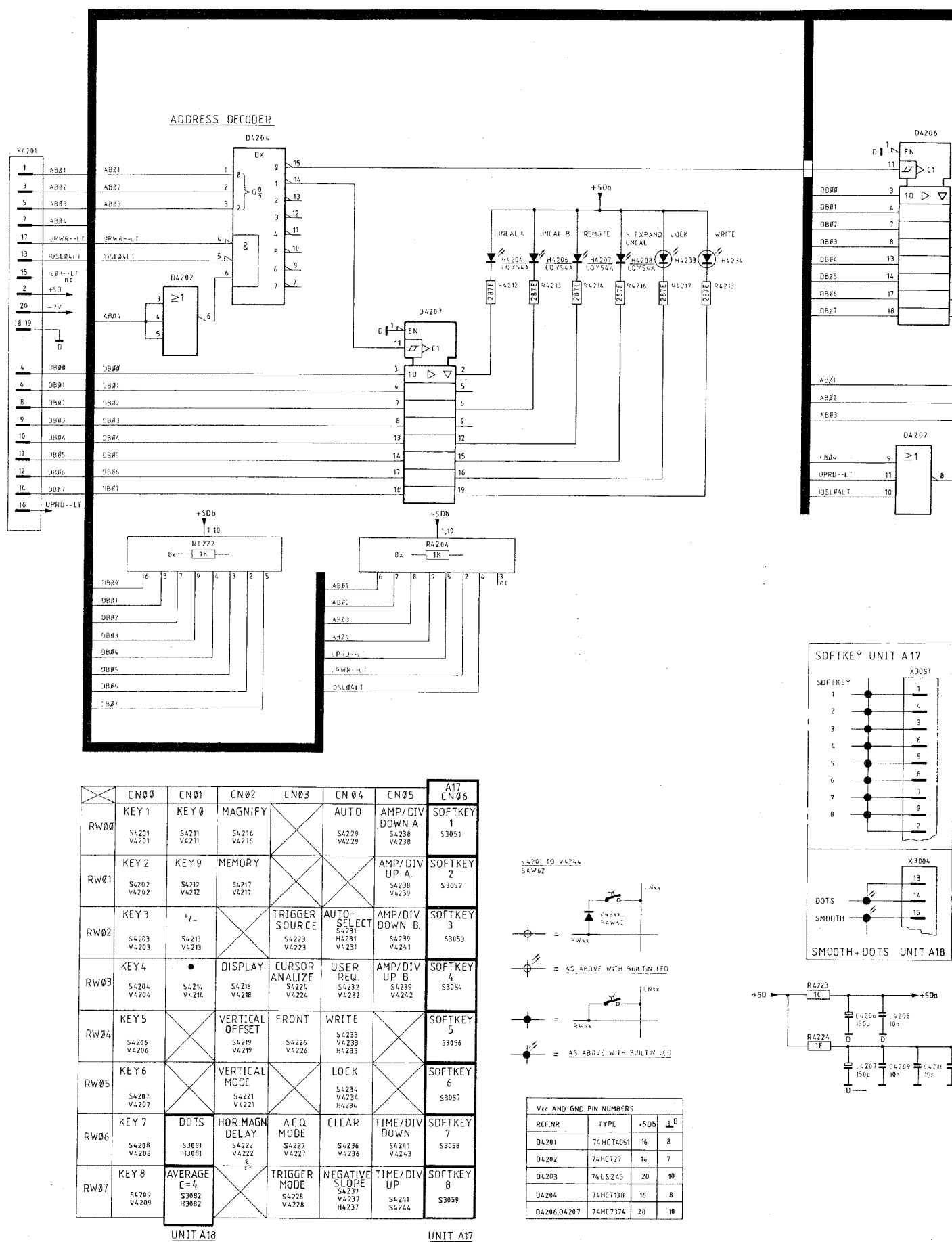


Figure 8.13.2 Unit A13 - FRONT 1 - circuit diagram.

