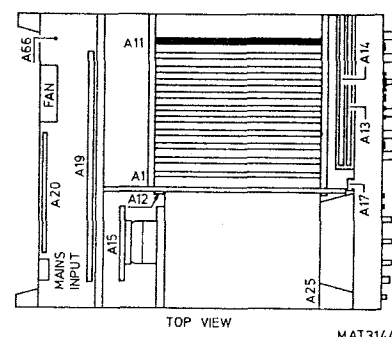


UNIT A11 - ADC + T&H UNITCONTENTS

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8.11.1 General information

The ADC and T&H unit accepts the samples from both input channels from the Vertical Signal unit A55 and converts these samples into 12 bits binary codes, which are routed to the DPU (unit A9) for further digital processing.

8.11.2 Circuit description

The samples from the Vertical Signal unit A55 are applied to the CORRECTION CIRCUIT.

Because jumper X608 is placed in position 1-2 in this instrument, the CORRECTION CIRCUIT operates as a linear amplifier. Potentiometer R721 has no function. The circuit controlled by transistor V622 is not active, due to the connection between the base and the emitter of V622.

The output signal at pin 15 of IC D616 is applied to a T&H gate (D613 and associated circuitry) via R707.

This T&H tracks the input signal continuously until the signal STCV-1 goes high. Now the output of D613 (pin 12) is held at the momentary value of the input signal.

Its output voltage goes via a buffer amplifier (V607, V608 and V609) to another buffer amplifier; N601 and associated components.

From this buffer amplifier the signal (THOTAN) goes to the ADC.

This buffer amplifier gives a feedback in the track mode (N601 pin 10) to the T&H gate. It is also a separation between the ADC and the T&H gate.

The signal THOTAN is applied to the ADC.

The ADC starts the conversion on the STAD--HT signal from the ADC logic. During this conversion the T&H gate is in the hold mode, to give the ADC a stable input signal.

The ADC output lines ADOT00...ADOT10 are led to the overflow detection circuit and to the sample data latch.

Line ADOT11 is buffered by D607. The three buffered lines ADOT11-1...ADOT11-3 are led to the overflow detection and the code converter.

The overflow detection detects whether all 11 ADC output signals are "0" (sample voltage too negative) or "1" (sample voltage too positive). The outputs (wired or) generate via D609 (pin 12 and 9) the OFAD signal to the DPU (unit A9) to indicate that an overflow occurred during the conversion.

The code converter inverts ADOT11-3 (MSB) to convert the ADC output from straight binary code to two's complement code. This two's complement code is latched by the sample data latch and afterwards applied to the DPU by the OTDIAD signal from the DPU.

The ADC logic generates the control signals from the UPCK16 signal. Figure 8.11.1 shows the timing diagram.

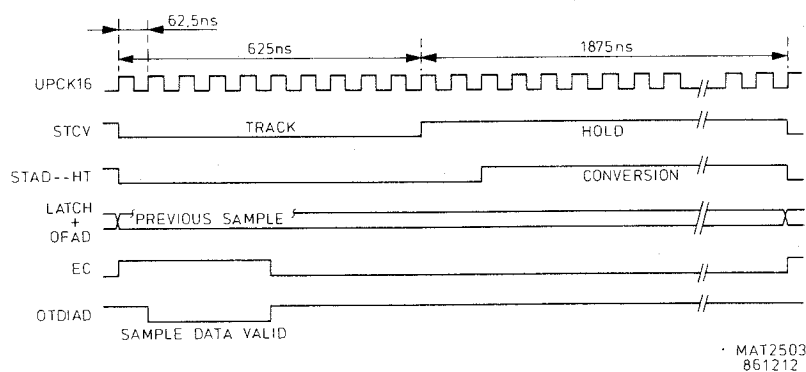


Figure 8.11.1 Timing diagram of the ADC and T&H unit.

8.11.3 Signal name list

UNIT A11

Signal name	Description	Signal source	Signal destination(s)
ADOT00...ADOT11	ADC out 00...11	A11	A11
ADOT11-1...11-3	ADC out 11-1...11-3	A11	A11
CDRSMO	(no function)	A8	-
EC	End of conversion	A11	A12-A8
	oscillator	A25	-
OFAD	Overflow ADC	A11	A12-A9
OTDIAD	Output disable ADC	A8	-
SADB00...11	Sample data bus 00...11	A11	A12-A9
STAD--HT	Start ADC	A11	A11
STAD--LT	Start ADC	A11	A11
STCV	Start conversion	A5	-
THINAN	Track & Hold in analogue	A55	-
THOTAN	Track & Hold out		
	analogue	A11	A11
UPCK16	Microprocessor clock		
	16 MHz	A6	-

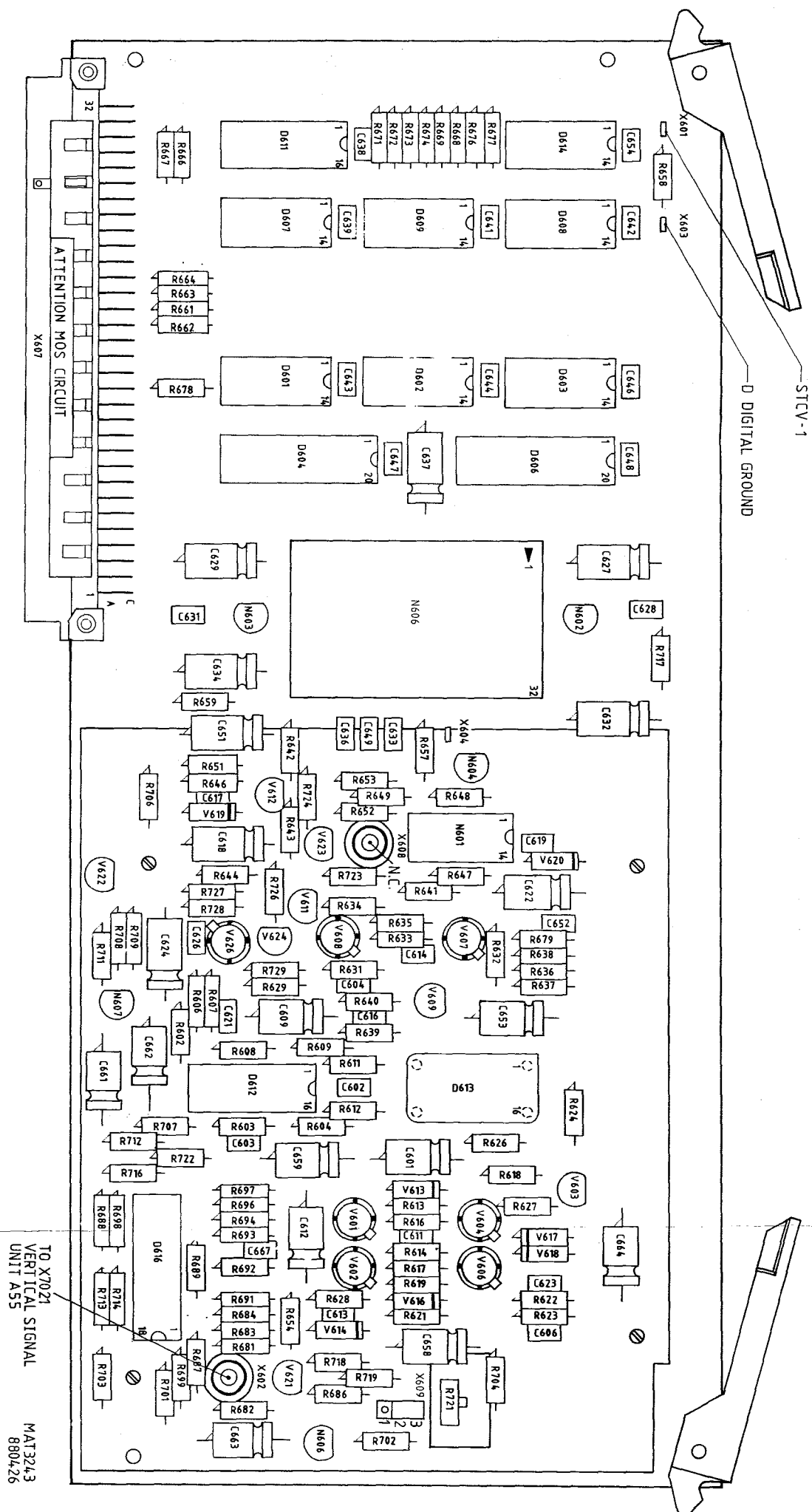
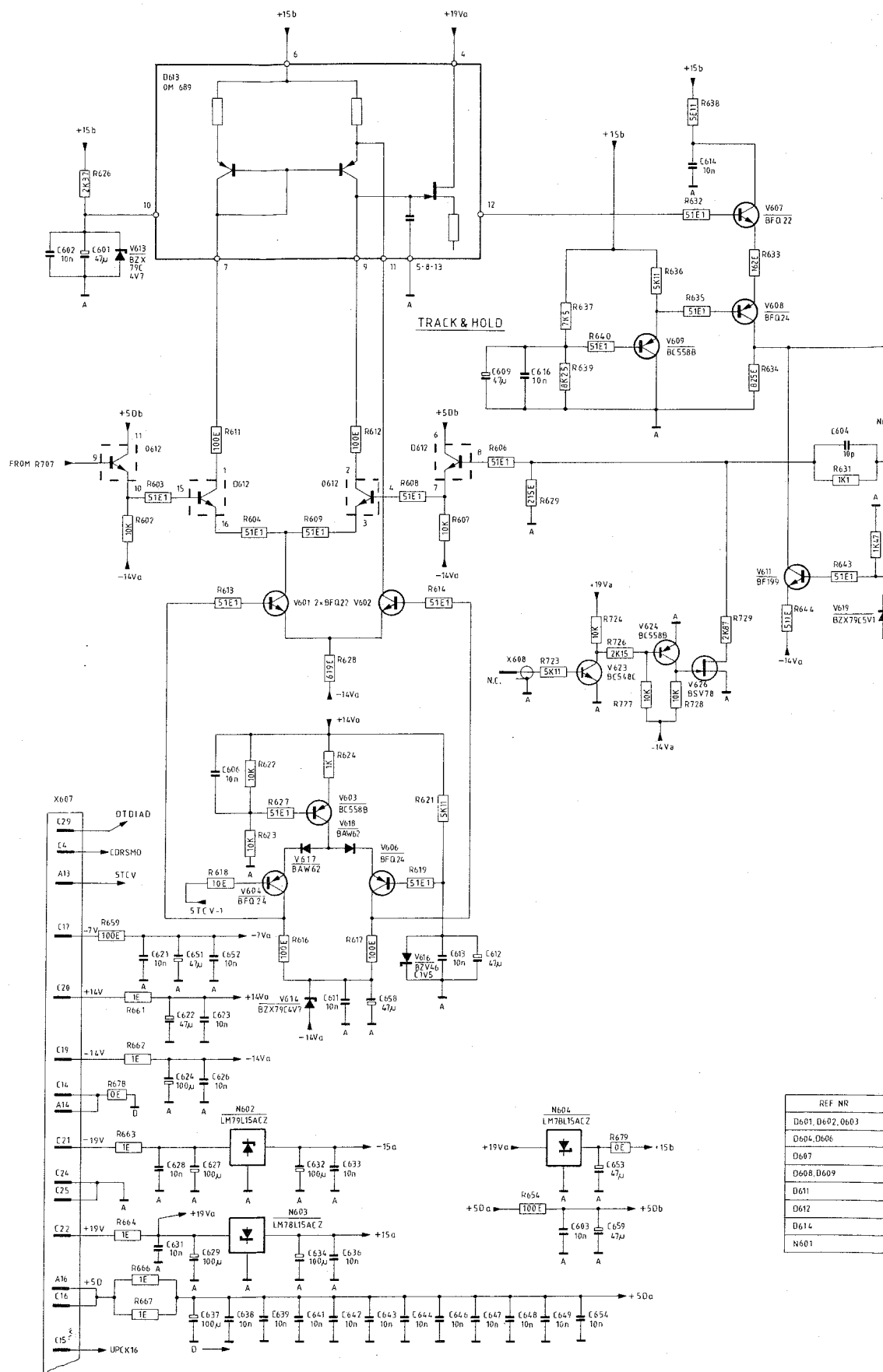


Figure 8.11.2 Unit A11 - ADC + T&H UNIT - p.c.b. lay-out.

TO X7021
VERTICAL SIGNAL
UNIT A55

MAT3243
880426



REF NR
D601, D602, D603
D604, D606
D607
D608, D609
D611
D612
D614
N601

