

## **CIRCUIT DESCRIPTIONS**

**8**

## CIRCUIT DESCRIPTIONS

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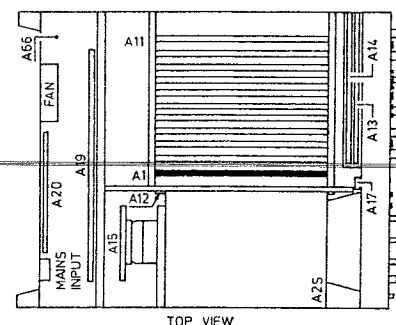
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## 8.0 CIRCUIT DESCRIPTIONS

The functioning of the circuit is explained in this chapter. It is done per unit and in unitnumber (A..) sequence.

Every unit section contains a circuit description, the lay-out of the p.c.b., the circuit diagram(s) and a signal-name list.

See also chapter 7.0 "INTRODUCTION TO CIRCUIT DESCRIPTIONS".

UNIT A1 - FINAL AMPLIFIER UNIT

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## 8.1.1 General information

This unit basically comprises the vertical and horizontal final amplifiers, the overscan detection circuit, the Z-amplifier, the calibrator circuit and the analog plot interface.

## 8. 1.2 Vertical final amplifier

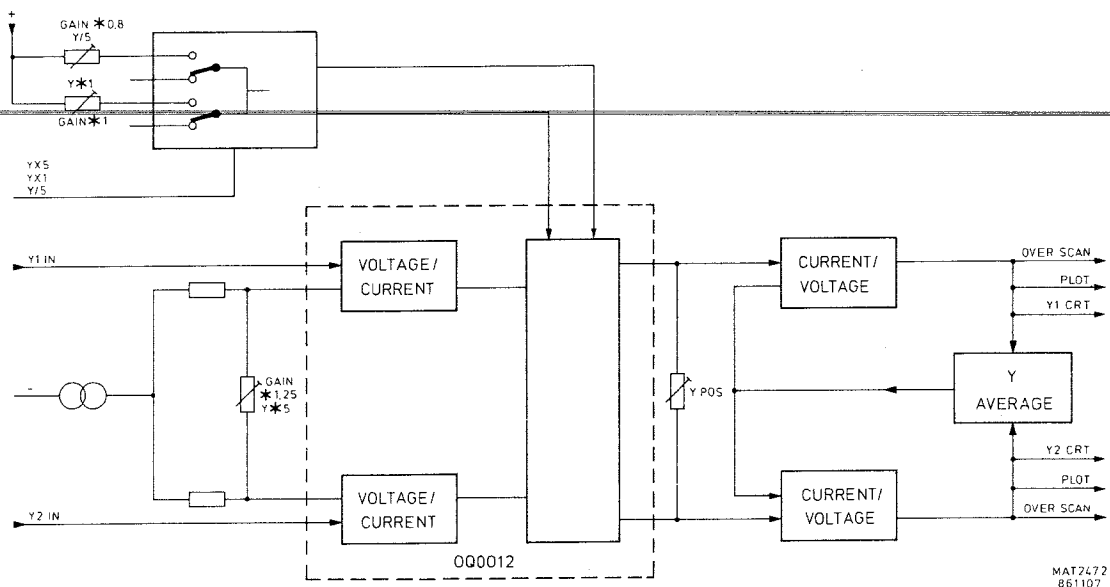


Figure 8.1.1 Blockdiagram Y-final amplifier.

The output signals Y1IN and Y2IN from the DISPLAY DAC UNIT A2 are applied to a voltage/current converter of which the x1,25 (Y\*5-mode) gain can be adjusted by potentiometer R2531 in the emitter circuit of the input transistor of D2507.

Furthermore, the gain can be influenced for the Y\*1 and the Y/5 mode. Two sections of multiplexer D2501 can be switched by the signals ANEPY-HT (analog expand) and ANCPY-HT (analog compress) from DISPLAY CONTROL UNIT A3.

The switching is done according the following table:

MODE	ANCPY-HT	ANEPY-HT	analog expand factor (UNIT A1)	digital expand factor (UNIT A2)
Y/5	1	0	x0,8	/4
Y*1	0	0	x1	x1
Y*5	0	1	x1,25	x4

An additional circuit can be switched in for the x1 gain (adjustable with potentiometer R2513) and an additional circuit can be switched in for the x0,8 gain (adjustable with potentiometer R2516). The selection depends on the user selection of the Y\*5, Y\*1 or the Y/5 mode.

Output points 12/13 and 14/15 of the MULTIPLIER D2506 are applied to current/voltage converters in the Y-OUTPUT stage of which the balance can be adjusted by potentiometer R2533.

The average value of the signals Y1 and Y2 is fed back to the input of the X-OUTPUT stage to keep the average value constant.

The signals X1 and X2 are applied to the vertical deflection plates of the C.R.T., to the OVERSCAN DETECTION circuit on unit A1 and also to the PLOT INTERFACE on this unit A1.

## 8.1.3 Horizontal final amplifier

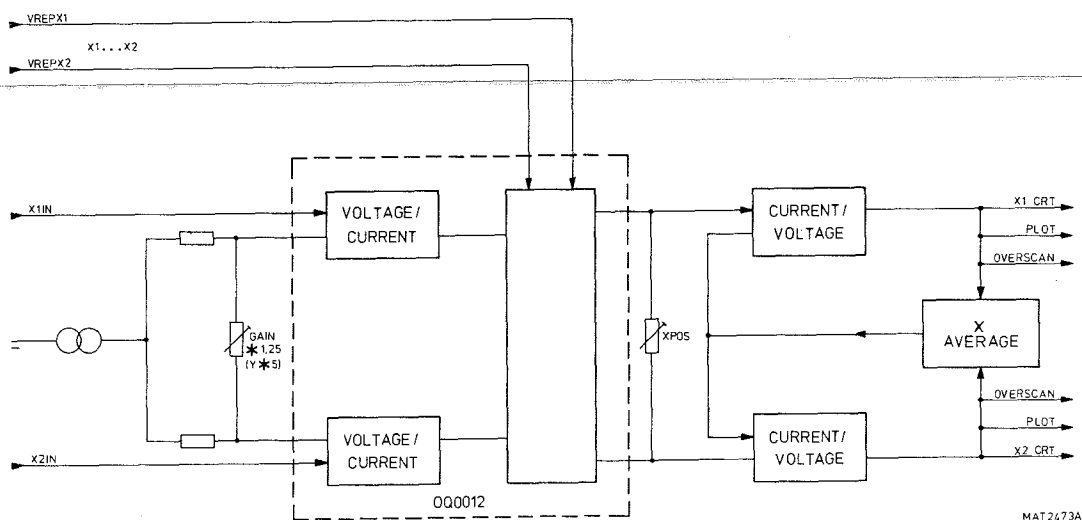


Figure 8.1.2 Blockdiagram X-final amplifier.

The output signals X1IN and X2IN from the DISPLAY DAC UNIT A2 are applied to a voltage/current converter of which the x1 gain can be adjusted by potentiometer R2566 in the emitter circuit of the input transistors of D2507.

Furthermore, the gain can be influenced by signals VREPX1 and VREPX2 which carry a variable X-EXPAND factor between x1/2 (EXPAND x1) and x1 (EXPAND x2). This factor, which is user selected, is multiplied in the stage D2507 to vary the X-gain.

Output points 12/13 and 14/15 of the MULTIPLIER D2507 are applied to current/voltage converters in the X-OUTPUT stage of which the balance can be adjusted by potentiometer R2571.

The average value of the signals X1 and X2 is fed back to the input of the X-OUTPUT stage to keep the average value constant.

The signals X1 and X2 are applied to the horizontal deflection plates of the C.R.T., to the OVERSCAN DETECTION circuit on unit A1 and also to the PLOT INTERFACE on this unit A1.

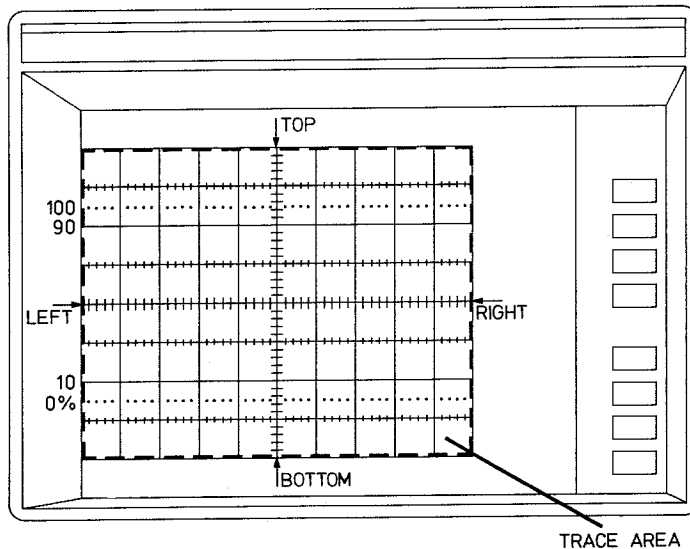
## 8.1.4 Trace/Text intensity

The levels ITTR from the TRACE INTENS frontpanel control and ITTX from the TEXT INTENS frontpanel control on C.R.T. CONTROL UNIT A16, are applied to one section of multiplexer D2501. This section, which is switched by the signal DPTR--HT (display trace), switches the trace intensity level to the Z-amplifier when traces have to be displayed and the text intensity level when texts have to be displayed.

8.1-4

#### 8.1.5 Overscan detection

The output signals Y1, Y2, X1 and X2 from the vertical and horizontal final amplifiers are applied to an overscan detection circuit where they are compared with four overscan levels for the top, bottom, left and right sides of the trace area on the C.R.T. screen.



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Figure 8.1.3 Overscan detection.

These levels can be adjusted by potentiometers R2658, R2659, R2678 and R2682 in such a way that during the display of traces, the traces can never be displayed outside the trace area on the C.R.T. screen. In case of overscan a blanking signal is produced by the collector of transistor V2623 and this signal is applied to the Z-amplifier to blank the trace.

The overscan detection circuit can be disabled during text display and enabled during trace display by the signal DIOS--HT (disable overscan) via transistor V2611.

## 8.1.6 Z-amplifier

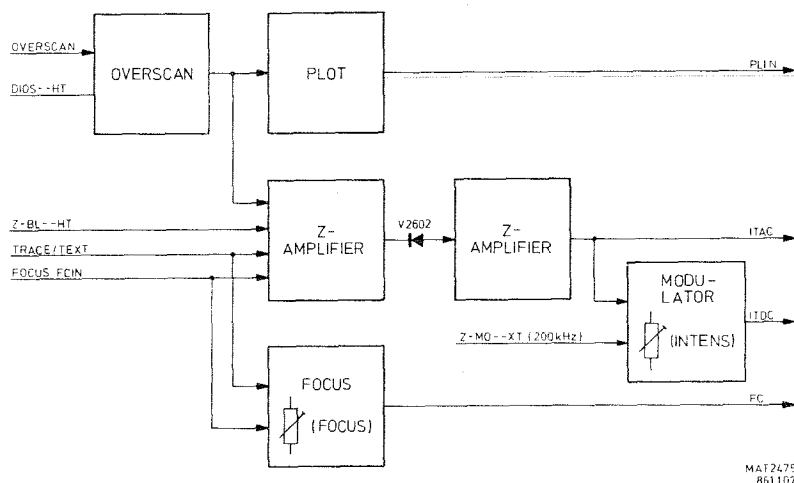


Figure 8.1.4 Blockdiagram Z-circuit.

INTENS

The Z-circuit is controlled by a number of different inputs:

- Overscan
- Z-blank signal
- TRACE or TEXT intensity control level
- FOCUS control level

The signals are applied to a Z-amplifier and the output of this amplifier is guided along two different signal path's. A high frequency component signal path (signal ITAC) and a low frequency component signal path (signal ITDC).

Signal ITAC is directly applied to Z-AMPLIFIER UNIT A15 and from there via a high voltage capacitor to the high voltage part of the circuit and to the intensity grid G1 of the C.R.T..

The low frequency component is applied to a modulation circuit, it can be influenced by a fine adjusting potentiometer R2637 and afterwards modulated with a frequency of 200 kHz from signal Z-MO--XT from the clock generator on the uP unit A6.

The resulting signal ITDC is applied to Z-AMPLIFIER unit A15 and via Z-circuit transferred via a high voltage capacitor to the high voltage part of the circuit. It is then demodulated, combined with the high frequency component and applied to the intensity grid G1 of the C.R.T..

FOCUS

The FOCUS circuit is influenced by the setting of the front panel FOCUS controls as well as the setting of the TRACE and TEXT intensity controls. The last is needed for the auto focus control when the intensity is changed with one of the frontpanel TRACE or TEXT intensity controls. There is also a fine adjustment potentiometer R2609.

The resulting signal FC is applied to the focus circuit on Z-AMPLIFIER UNIT A15 and from there to the focus grid G3 of the C.R.T..

8.1-6

8.1.7 Calibrator

This calibrator circuit is not used in this instrument.  
The calibrator can be found on the Distribution unit A53 (see section 8.53).

8.1.8 Plot interface

The output signals Y1, Y2, X1 and X2 from the vertical and horizontal final amplifiers are applied to a plot interface where they are prepared to be plotted via the rear panel analog plot output socket.

The X-output gain can be adjusted with potentiometer R2728 and the Y-output gain with potentiometer R2738.  
Sample and hold signal SAPL activates the interface for a plot action. Signals are only applied to the output socket when enabled by signal PLZEOT if a value is stored in the sample and hold circuit.

A pen lift circuit is activated via the PLIN signal (when an overscan is detected). The penlift flip flop can be reset by the PEN UP signal PU----LT.

The pen lift polarity can be influenced by signal PFPY via exclusive or circuit D2504.

## 8.1.9 Signal-name list

UNIT A1

Signal name	Description	Signal source	Signal destination(s)
ANCPY-HT	Analog compress Y	A3	-
ANEPY-HT	Analog expand Y	A3	-
DIOS--HT	Disable overscan	A3	-
DPTR--HT	Display trace	A3	-
FC	Focus	A1	A15
FCIN	Focus input	A16	-
ITAC	Intens a.c. component	A1	A15
ITDC	Intens d.c. component	A1	A15
ITTR	Intensity trace	A16	-
ITTX	Intensity text	A16	-
PENLIFT	Penlift	A1	A66
PLIN	Plot input	A1	A1
PFPY	Penlift polarity	A3	-
PLZEOT	Plot zero output	A3	-
PU----LT	Pen-up	A3	-
SAPL	Sample plot	A3	-
X1	X1 input for C.R.T.	A1	A15-C.R.T.
X2	X2 input for C.R.T.	A1	A15-C.R.T.
X1IN	X1 input final amplifier	A2	-
X2IN	X2 input final amplifier	A2	-
X-PL	X plot	A1	A66
Y1	Y1 input for C.R.T.	A1	A15-C.R.T.
Y2	Y2 input for C.R.T.	A1	A15-C.R.T.
Y1IN	Y1 input final amplifier	A2	-
Y2IN	Y2 input final amplifier	A2	-
Y-PL	Y plot	A1	A66
VREPX1...X2	Variable expand X	A2	-
Z-BL--HT	Z-blanking	A3	-
Z-MO--XT	Z-modulation (200 kHz)	A6	-

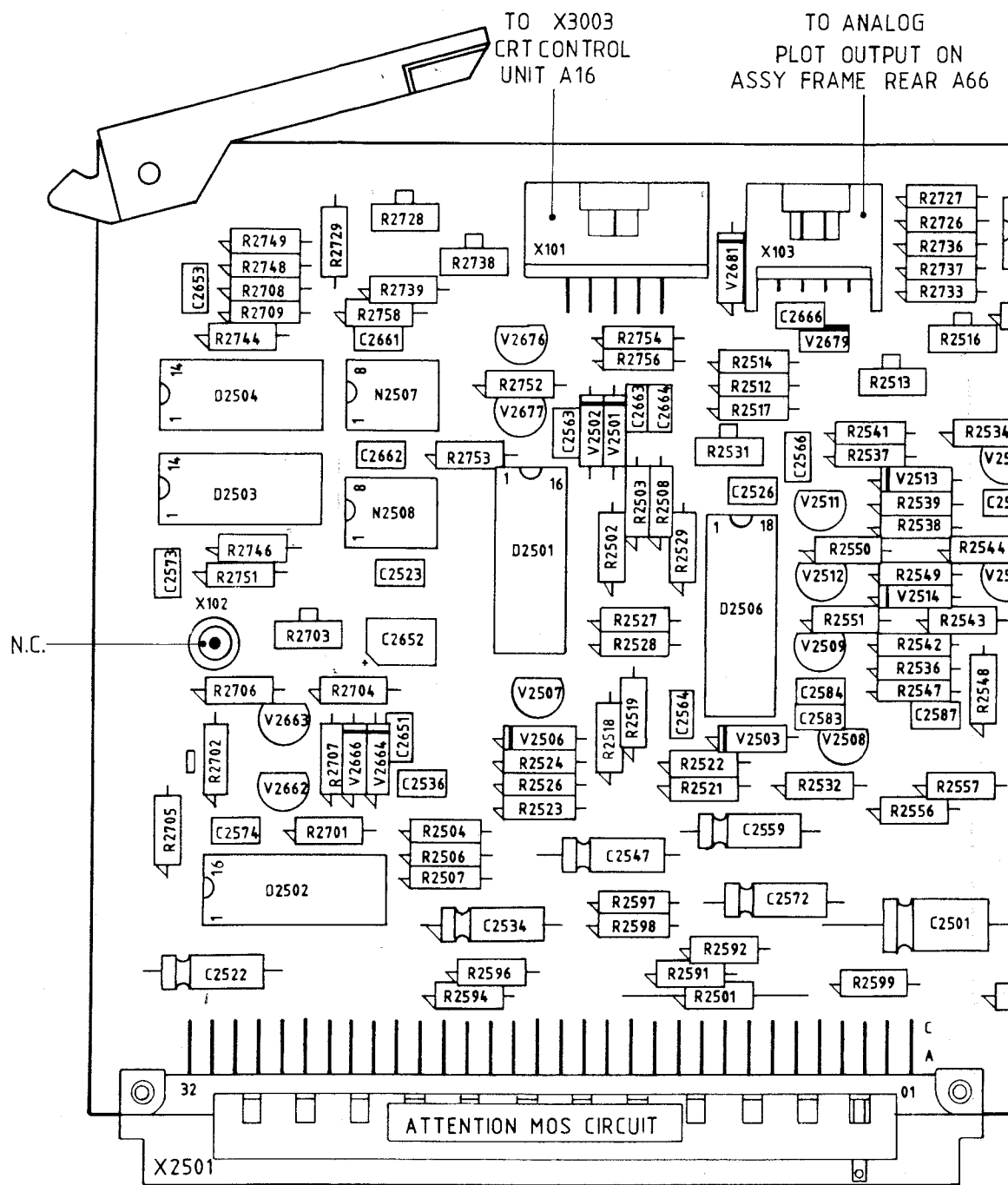
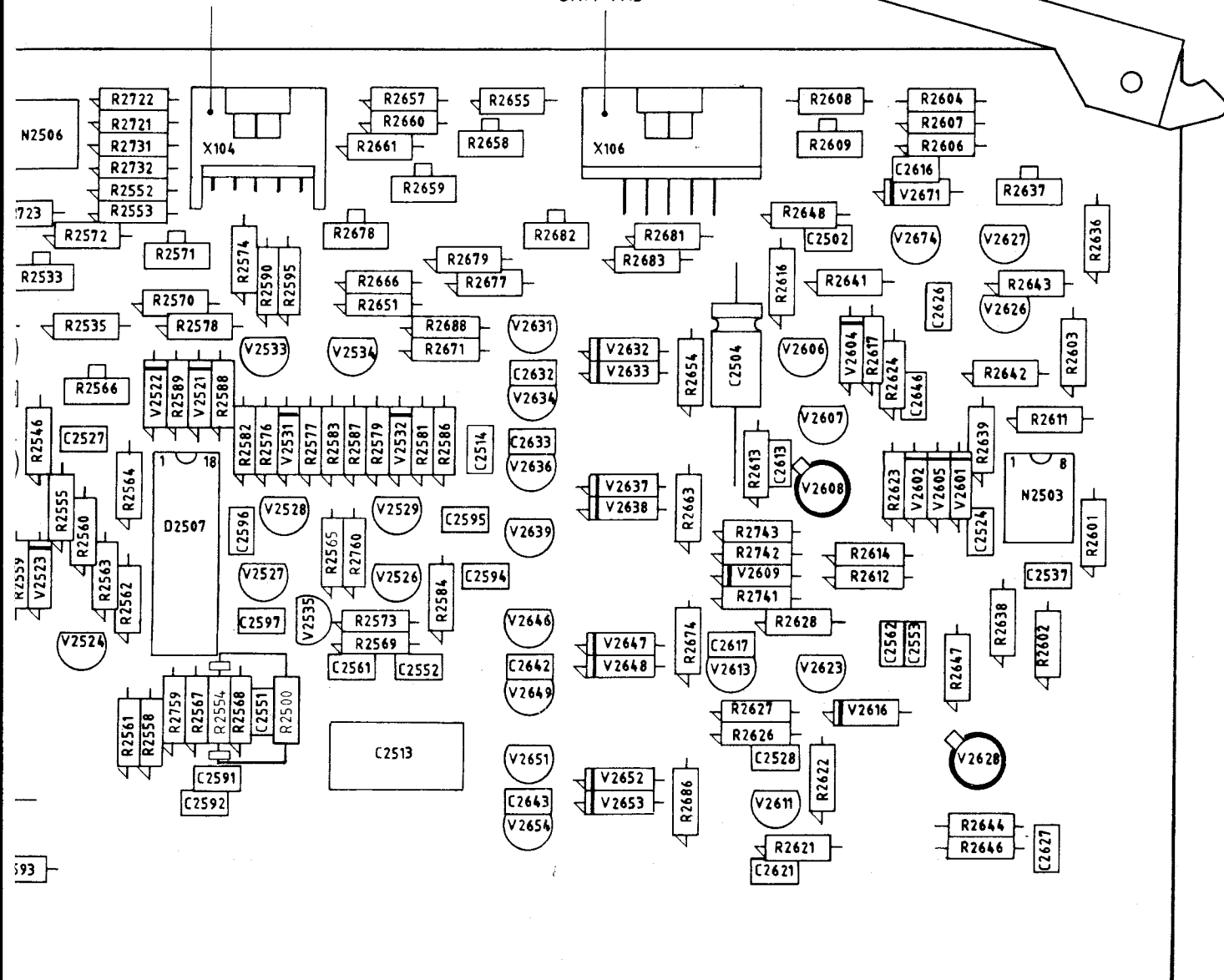


Figure 8.1.5 Unit A1 - FINAL AMPLIFIER UNIT - p.c.b. lay-out.

TO X1502  
Z-AMPLIFIER  
UNIT A15

TO X1501  
Z-AMPLIFIER  
UNIT A15



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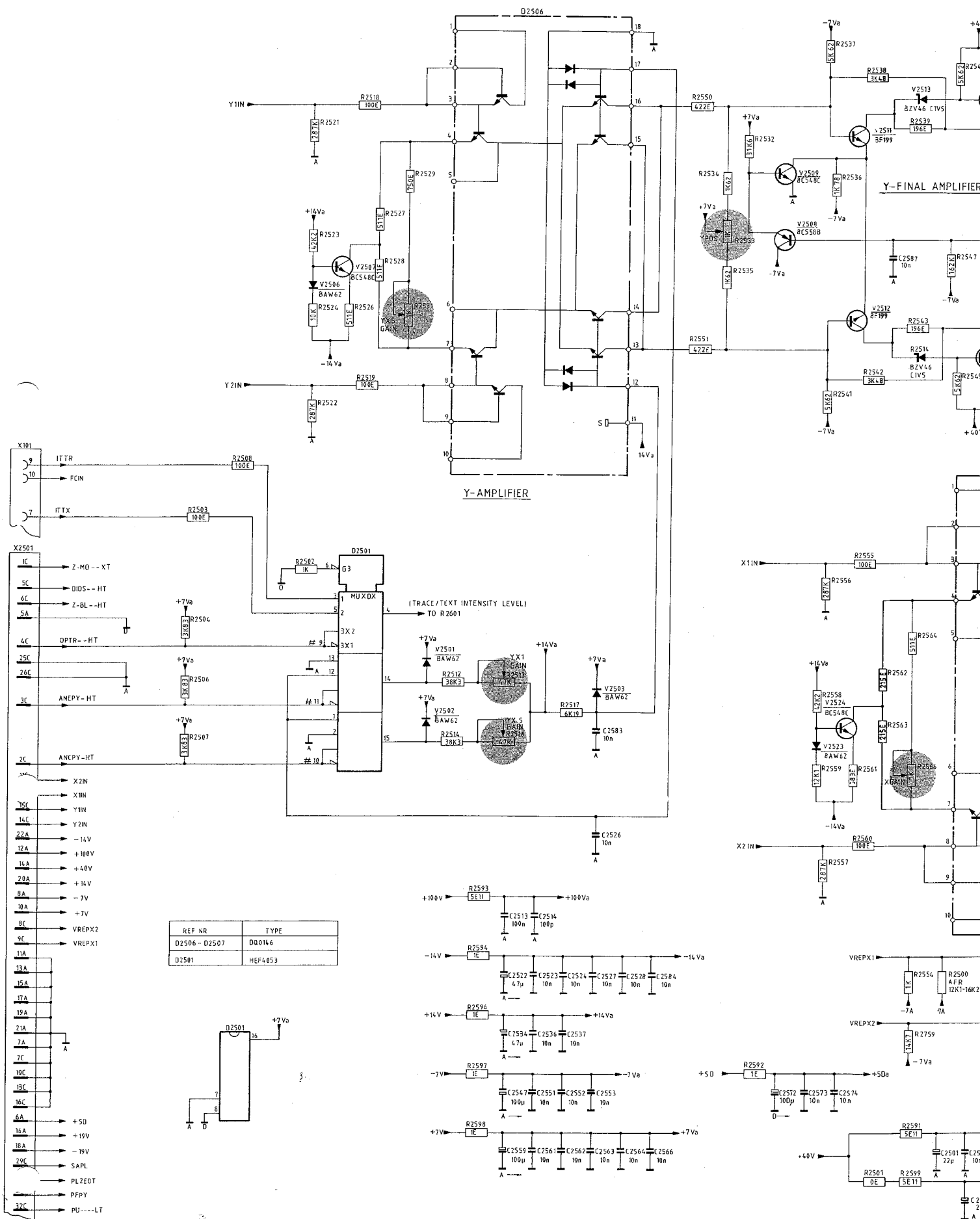
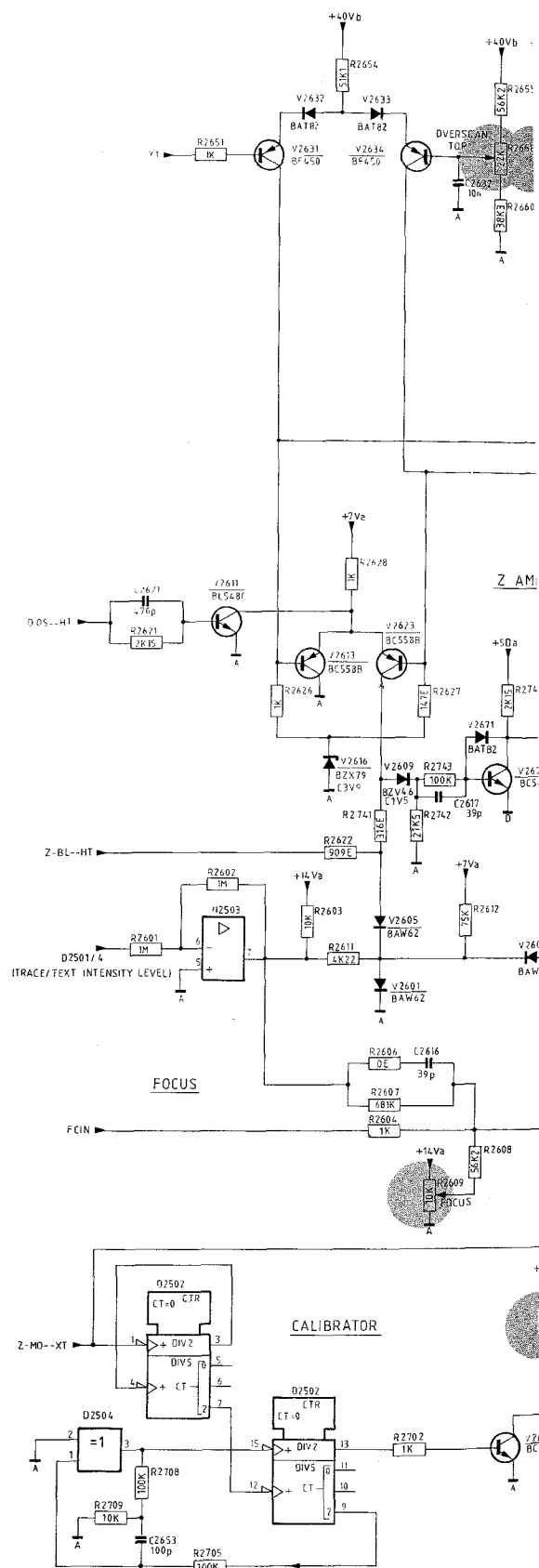
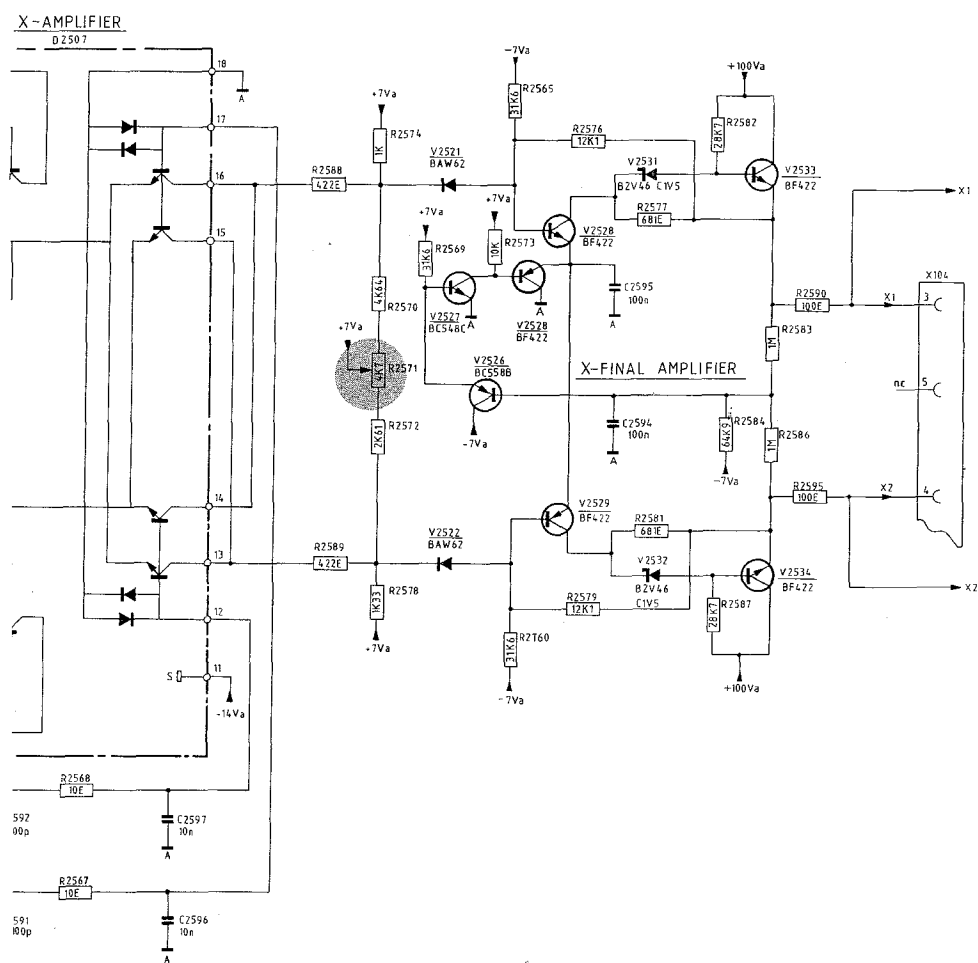
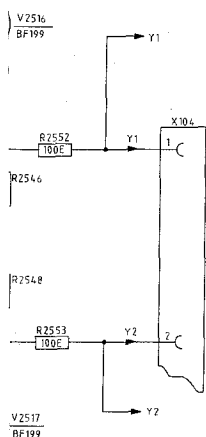


Figure 8.1.6 Unit A1 - FINAL AMPLIFIER UNIT - circuit diagram.





REF NO	
D2502	
D2503	
D2504	
N2503	
N2506	
N2507	N2508

