

## **BLOCKDIAGRAM AND DESCRIPTION**

**6**

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## 6.0 BLOCKDIAGRAM AND DESCRIPTION

This chapter serves to explain the main functions of the oscilloscope. The system can be divided into a number of sections:

- Acquisition section
- Calculation section
- Display and plot section
- Front section
- Control section
- Power supply section

### 6.1 ACQUISITION SECTION

By means of the acquisition section the analog signals are sampled and converted into digital codes.

Before conversion the analog input signals must be adapted so that an Analog to Digital Converter (ADC) is able to convert them.

#### 6.1.1. The vertical channels (units A54...A57, A69).

The vertical section consists of two identical channels A and B with a sensitivity range of 1 mV/div...200 mV/div in a 1-2-5 sequence. Each channel includes a probe indication. Since both channels are identical, only channel A is described.

The input signal is applied to the SAMPLING GATE via a TRIGGER PICK-OFF and a 30 nsec DELAY LINE.

The TRIGGER PICK-OFF supplies a trigger signal with an amplitude of about one tenth of the input signal to the TRIGGER INPUT unit.

The DELAY LINE compensates the time delay in the trigger circuits, which enables the trigger point to be displayed on the screen.

The SAMPLING GATE takes samples of the input signal on receipt of a sampling pulse from the SAMPLING DRIVER, which gets the sampling pulses on its turn from the FAST RAMP unit.

The SAMPLING GATE is supplied by the AVALANCHE VOLTAGE circuit and the SNAPP OFF CURRENT circuit. The samples are first amplified by the PRE-AMPLIFIER and the AMPLIFIER of which the amplification factor is depending on the selected vertical sensitivity of the instrument. The TRACK & HOLD circuit, which is controlled by the TRACK & HOLD CONTROL holds the samples for a while.

Next the samples go via the VARIABLE circuit to the CHANNEL SWITCH. This switch selects channel A or channel B or switches between them if both channels are selected.

Via the BRIDGE, the selected OFFSET and the feedback signal from the FEEDBACK ATTENUATOR are added to the input signal.

The feedback attenuation factors and the amplification factors are set by the microprocessor via the VERTICAL LATCH.

### 6.1.2 The management circuit (unit A25).

The feedback codes from the DPU are converted from 2's complement code to straight binary code by CODE CONVERT and applied to FEEDBACK LATCH A and FEEDBACK LATCH B.

Via the FEEDBACK DAC, which converts to an analog signal and a multiplier VARIABLE, the feedback signal is applied to the VERTICAL SIGNAL unit.

The CHANNEL SWITCH DRIVER buffers the channel switch control signal.

Data from and to the microprocessor are buffered by the BIDIRECTIONAL DATA BUFFER.

The address bus is buffered by the ADDRESS BUFFER, which is controlled by the I/O SELECT DELAY. The ADDRESS DECODER selects one of the STATUS FLIPFLOPS and the INPUT PORT. Via the STATUS FLIPFLOPS, the microprocessor sets the hardware corresponding to the settings made on the front panel.

Via the INPUT PORT the probe type information is read from the PROBE DETECTION circuit on the DISTRIBUTION unit. Also a number of trigger status signals are read via this port.

Four DACs supply the offset signals to the VERTICAL SIGNAL unit. These DACs are: OFFSET DAC FINE A, OFFSET DAC COARSE A, OFFSET DAC FINE B and OFFSET DAC COARSE B.

### 6.1.3 The ADC circuit (unit A11)

Signal levels from the CHANNEL SWITCH are applied via a CORRECTION CIRCUIT to a TRACK AND HOLD circuit which is able to hold the levels for a time long enough for the ADC circuit behind it to do the conversion to a 12-bit digital word. The ADC is able to perform conversion in 2.5  $\mu$ s and is controlled by the ADC LOGIC. The 12-bit digital code is converted from straight binary into two's complement by the CODE CONVERT circuit and then latched in the SAMPLE DATA LATCH for further data handling by the Digital Processing Unit (DPU). The ADC output is also connected to an OVERFLOW DETECTION circuit, which on its turn is connected with the DPU.

### 6.1.4 The trigger circuits (units A31, A32 and A34)

The signals from the TRIGGER PICK-OFFS and an EXTERNAL trigger signal are applied to the TRIGGER SELECTOR on the TRIGGER INPUT unit. The selected trigger signal is led via the X1/X10 AMPLIFIER to the PRESCALER, which is used for the count down mode.

The TRIGGER AMPLITUDE DETECTOR detects if the amplitude of the trigger signal is sufficient for triggered mode or count down mode.

The trigger signal from the PRESCALER is applied to the BUFFER on the THREE STAGE TRIGGER unit.

Via the SLOPE CONTROL, the trigger signal is led to the three stages STAGE 1, STAGE 2 and STAGE 3. Via LEVEL CONTROL these stages receive a trigger level signal.

After the HOLD OFF time being elapsed, which is marked by a signal from the SYNC SWITCH on the FAST RAMP unit, the three stages change over in sequence on receipt of a trigger signal, resulting in a signal from STAGE 3, which starts the FAST RAMP GENERATOR on the FAST RAMP unit.

In synchronized mode, the stages are released continuously via the SYNC CONTROL, which results in a signal to the FAST RAMP GENERATOR, directly after the hold off time.

The trigger signal from the TRIGGER INPUT unit is applied via a FILTER/AMPLIFIER, to the DIVIDER HIGH AMPLITUDE and the DIVIDER LOW AMPLITUDE. Their output signals are used for the trigger mode control by the UPPER FREQUENCY DETECTOR, the LOWER FREQUENCY DETECTOR, the COUNT DOWN CONTROL and the TRIGGER MODE CONTROL. The microprocessor determines the triggermode via the TRIGGER LATCH. The TRIGGER LEVEL ADAPTION adapts the signal from the TRIGGER LEVEL DAC on the Management unit for the Three Stage Trigger unit.

#### 6.1.5 The time-base circuits (units A51 and A52)

When a trigger occurs, a signal from STAGE 3 on the Three Stage Trigger unit starts the FAST RAMP GENERATOR. When the signal crosses the level of the stair signal from ADD INVERT, the FAST RAMP/STAIR COMPARATOR generates a sampling pulse, which is applied to the SAMPLING DRIVER.

This causes a sample of the input signal to be taken. There is also a sampling signal applied to the Acquisition Control Logic on the GRAM unit.

When the fast ramp reached its end level, the END OF FAST RAMP COMPARATOR sets the HOLD OFF FLIPFLOP, which on its turn blocks further trigger pulses from the Three Stage Trigger unit via the SYNC SWITCH. The Three Stage Trigger unit also resets the FAST RAMP GENERATOR.

When the HOLD OFF FLIPFLOP is set, the HOLD OFF INTEGRATOR is started. The slope of the output signal is determined by the microprocessor, via the HOLD OFF DAC. The end level of this signal is determined by the END OF HOLD OFF COMPARATOR, which resets the HOLD OFF DAC.

The stair signal, which is used for the sequential sampling system, is generated by the STAIR COUNTER and the STAIR DAC. After every sample, the Acquisition Control Logic on the GRAM generates a count pulse to the STAIR COUNTER. The binary value of the output signal is incremented, which result in an increase of the output signal of the STAIR DAC.

To obtain a trigger delay this signal can be attenuated by the STAIR ATTENUATOR and a d.c. signal from the TRIGGER DELAY DAC can be added to it, before it is inverted in the ADD INVERT circuit.

Via the TIME-BASE LATCH, the Microprocessor controls various settings on these units, depending on the selected front panel settings. It also controls the slope of the fast ramp via the FAST RAMP DAC.

#### 6.1.6 The acquisition control logic (unit A5)

The ACQUISITION CONTROL LOGIC (ACL) controls the timing of the acquisition system.

Via the ACL LATCH it is informed by the microprocessor about the selected front panel settings. The ACL RESET LOGIC resets the ACL under control of the IL01--LT signal from the microprocessor or TRRY from the DPU Control.

## 6.2 THE CALCULATION SECTION (units A8 and A9)

The calculation section consists of a Data Processing Unit (DPU unit A9) which is a very fast microcomputer system with a cycle time of 125 nsec.

It takes data from the ADC, performs calculations on it and sends the data to the TRACE DATA LATCH and to the FEEDBACK LATCHES. All data are transported via the BUFFER.

The possible calculations are:

- adding of both channels in ADD mode
- inverting of one or both channels
- averaging
- linear interpolation
- overflow detection

To perform the calculations the DPU has a number of calculation registers and function blocks:

- REGISTER I, II and III
- SHIFT REGISTER
- +/- (complement function)
- ADDER
- LIMIT DETECTION

An overflow at the ADC is detected by the OVERFLOW DETECTION circuit, which enables the REFLECTION SUPPRESSION.

The DPU has registers in which data are stored. These are:

- PRE-TRIGGER RAM.  
This is used as general workspace, e.g. for interpolation calculations.
- AVERAGE RAM.  
Used for average calculations.
- FLAG RAM.  
In this ram is stored whether samples are real samples or samples obtained by interpolation. If an overflow occurs, this is also stored by means of a flag. Flags are stored by means of the FLAG HANDLER.

The DPU is controlled by the DPU control (unit A8). The heart of the DPU control is the CONTROL MEMORY. This serves as a program memory for the DPU.

This memory is loaded for the various functions by the microprocessor system via the ADDRESS MULTIPLEXER and the BUFFER.

The DPU control has a PIPELINE REGISTER, which holds the current instruction, while the next instruction is fetched from the CONTROL MEMORY.

The instruction which is fetched depends on the address given by the ADDRESS MULTIPLEXER.

This address depends on data given by the STATUS MULTIPLEXER, which on its turn gets status signals from various function blocks.

The PIPELINE REGISTER is controlled by the START/STOP logic and the CONTROL LATCH.

When a DPU program is finished, the START/STOP LOGIC informs the microprocessor system about this via interrupt line IL02--LT.

The INSTRUCTION REGISTER and the CONTROL REGISTER, control the operation of the DPU control.

The ADDRESS GENERATOR generates addresses for the PRE TRIGGER RAM, the AVERAGE RAM and the FLAG RAM.

The ADDRESS GENERATOR consists of an ADDRESS REGISTER and a PRETRIGGER COUNTER, which can be loaded via a buffer. The MULTIPLEXER selects the ADDRESS from the PRETRIGGER COUNTER or from the ADDER. The ADDER adds the addresses from the ADDRESS REGISTER and the OFFSET JUMP REGISTER. The latter enables the DPU to make jumps in program execution.

The TRIGGER ADDRESS COMPARATOR has no function in this instrument.

The ADDRESS DECODER enables the microprocessor system to have control over the calculation section.

### 6.3 DISPLAY AND PLOT SECTION (units A1, A2, A3 and A4)

The display section consists of hardware to display trace data as well as text data on the C.R.T display.

A complete display cycle for all traces and all texts to be displayed, is realized in less than 20 ms. This results in a stable and flicker-free display.

Trace data words from the DPU system which have to be copied to the TRACE MEMORY in the display section are latched in the TRACE DATA LATCH in the rhythm of the DPU clock and the display section is for each new trace data word informed via the HANDSHAKE LOGIC (signal sample ready) that it is available for storage in REGISTER R0 of the TRACE MEMORY.

Addresses for the TRACE MEMORY are then generated by the COPY ADDRESS COUNTER. This counter which is corrected to the TRACE MEMORY via ADDRESS MULTIPLEXER II starts each new copy cycle for a complete new trace with the generation of address zero. It counts then by the same rhythm as the DPU. After the storage of each trace data word in the TRACE MEMORY, a sample ready acknowledge signal is given to the DPU via the HANDSHAKE LOGIC.

#### 6.3.1 The SAVE function

When a SAVE function is selected, the contents of REGISTER R0 is copied in one or more of the REGISTERS R1, R2 or R3.

The trace data words are then first saved in the SAVE LATCH before they are saved in the selected REGISTER.

The REGISTER can be addressed then by the DISPLAY ADDRESS COUNTER via ADDRESS MULTIPLEXERS I AND II.

#### 6.3.2 Trace display

X=t display mode

The trace data words to be displayed are transferred from the TRACE MEMORY via the DISPLAY CONTROL LATCH to an INVERT stage which offers the facility to invert the stored data before display. This facility can be softkey selected per register.

Data passes then a VERTICAL EXPAND stage of which the expand factor is set in combination with the gain factor of the Y AMPLIFIER later in the signal path. In this way, the Y/5, Y\*1 and Y\*5 vertical expand modes are realized.

The resulting data are latched in a LATCH and vertical position information, which is calculated by the microprocessor and applied via a VERTICAL POSITION LATCH, can be added by a VERTICAL POSITION ADDER stage. It is then converted from 2's complement into straight binary by the CODE CONVERT circuit and latched in a YDAC LATCH before the

conversion by the digital to analog converter YDAC. The converter output signal can then be deglitched by a SAMPLE AND HOLD circuit and influenced by a DOT JOIN/SMOOTH circuit. It is then amplified by a Y AMPLIFIER by a factor which depends on the selected vertical expand factor. The signal is then applied to a Y FINAL AMPLIFIER which directly drives the vertical deflection plates of the C.R.T.

Horizontal deflection signals are derived from the addresses for the TRACE MEMORY, which are generated by the DISPLAY ADDRESS COUNTER. These addresses are applied via the DISPLAY ADDRESS DATA BUFFER to the HORIZONTAL EXPAND I CIRCUIT.

Horizontal expand factors of \*1, \*2, \*4 and \*8 can be realized. After expansion, horizontal position information, which is calculated by the microprocessor system and applied via a HORIZONTAL POSITION LATCH, can be added by a HORIZONTAL POSITION ADDER stage.

An additional expand factor of \*1 or \*8 can be realized in the HORIZONTAL EXPAND II circuit before the conversion by the digital to analog converter XDAC.

The converter output signal can then be deglitched by a SAMPLE AND HOLD circuit and influenced by a DOT JOIN/SMOOTH circuit. It is then amplified by an X AMPLIFIER of which the gain factor depends on the setting of the continuous X-EXPAND control on the frontpanel. This information is applied via an X-EXPAND LATCH and an X-EXPAND DAC to the X-AMPLIFIER.

The signal is then applied to an X FINAL AMPLIFIER which directly drives the horizontal deflection plates of the C.R.T.

#### A versus B display mode

This display mode is only selectable in dual channel mode.

The channel B TRACE MEMORY contents is applied to the vertical deflection plates of the CRT in a way as described for the X=t display.

For horizontal deflection the channel A TRACE MEMORY contents is used instead of the addresses from the DISPLAY ADDRESS COUNTER. The channel A trace data is converted from 2's complement into straight binary via the CODE CONVERT circuit and then transferred via the AVSB DATA BUFFER to the horizontal signal path and the horizontal deflection plates as described before for the X=t display addresses.

#### 6.3.3 Text display

The text which has to be displayed, is generated by the microprocessor system and stored in the TEXT MEMORY.

Data is transferred from the microprocessor data bus via the DATA/TEXT BIDIRECTIONAL LATCH to the TEXT MEMORY.

Addresses from the microprocessor address bus are applied to the TEXT MEMORY via ADDRESS MULTIPLEXER I.

Each dot to be displayed on the C.R.T screen is stored in the TEXT MEMORY by a word consisting of a vertical and a horizontal coordinate and an intensity flag.

There are a number of different text blocks like:

Top area text	(TAT)
Trace area text	(TRAT)
Bottom area text	(BAT)
Softkey text	(SKT)
Miscellaneous text	(MSC)

The vertical coordinates are applied to the vertical deflection plates of the C.R.T. via a TEXT/TRACE BIDIRECTIONAL BUFFER and in a way as described for the X=t display.

The horizontal coordinates are applied via the LINE TEXT DATA BUFFER (for TAT, TRAT and BAT) or via the SOFTKEY TEXT DATA BUFFER (for SKT) or via the AVSB DATA BUFFER (for MSC) to the horizontal signal path and the horizontal deflection plates as described before for the X=t display addresses.

The intensity flag is used to inform the Z-stage about normal or intensified display.

#### 6.3.4 Display control

Each display cycle, which consists of a fixed sequence of trace data blocks followed by a fixed sequence of text blocks, is controlled by the microprocessor system.

The microprocessor system places via a DATA BUFFER preset and control data into a number of OUTPUT PORTS, an Z + INTERRUPT TIMER and a PRESET REGISTER for the DISPLAY ADDRESS COUNTER, at the start of the display of each display data block.

At the same moment new position information is placed in the VERTICAL POSITION LATCH and in the HORIZONTAL POSITION LATCH.

At the end of each display block an interrupt signal IL05--LT is generated which is applied to the microprocessor system to ask for the actual preset and control data for the next display block.

#### 6.3.5 Z-control (unit A1 and A15)

The Z-AMPLIFIER is controlled by the following circuits:

- Reflection detection circuit
- Overscan detection circuit
- Z detection circuit

##### Reflection detection

Reflection is caused by adding a position information to a signal information in the vertical as well as in the horizontal signal path which causes an overflow in the highest (non-existing) bits. Such an overflow causes the top of the signal being displayed at the bottom of the display like it is a reflection. In a similar way an underflow causes a reflection in the top of the display. Both situations can also occur in horizontal direction. These reflection can be detected by the REFLECTION DETECTION circuit and via the Z-DETECTION circuit suppressed by the Z-AMPLIFIER.

### Overscan detection

Signals have to be displayed within the trace area of 8x10 divisions of the C.R.T. screen. Overscan in one of the four screen area directions is detected by the OVERSCAN DETECTION circuit and suppressed by the Z-AMPLIFIER.

### Z-detection

Via the Z-DETECTION which is controlled by the Z-TIMER circuit the trace will be blanked when no traces or texts have to be displayed. The text can also be intensified if required. The last, for example, for active functions.

The Z-DETECTION output signal is applied to the Z-AMPLIFIER where it is influenced by the INTENSITY controls for the trace as well as for the text. The resulting signal is applied via the final Z-AMPLIFIER to the Wehnelt Cylinder of the CRT thus controlling the intensity of the trace on the screen. The focussing of the trace is controlled via the FOCUS block, under the influence of a FOCUS control by a signal which is applied to the focus grid of the CRT.

The a.c. and d.c. components of the output blanking signal from the Z-AMPLIFIER are guided along different paths.

The a.c. path runs straight to the FINAL Z-AMPLIFIER via a high voltage capacitor.

The d.c. component is modulated with 200 kHz by a MODULATOR, guided via a high voltage capacitor to the high voltage part and demodulated again by a DEMODULATOR. The resulting components are added and applied to the FINAL Z-AMPLIFIER and from there to the Wehnelt cylinder of the C.R.T.

#### 6.3.6 Plot-output (unit A1)

Once per cycle of 20 ms a value can be plotted via the ANALOG PLOT INTERFACE. The X and Y informations are derived from the FINAL AMPLIFIERS and the penlift control is realized via the Z-AMPLIFIER stage.

#### 6.3.7 Option handling

For OPTION handling, e.g. like the Interface, the TRACE MEMORY as well as the TEXT MEMORY can be addressed via the microprocessor system address bus.

The data flows from the microprocessor system data bus to or from the TRACE MEMORY and the TEXT MEMORY is realized via the DATA/TEXT and TEXT/TRACE BIDIRECTIONAL latches.

#### 6.3.8 Calibrator (unit A53)

A CALIBRATOR generator generates a 100 kHz 1 Vp-p into 50 ohm calibration signal for the user which can be used to check the calibration of the system.

#### 6.4 FRONT SECTION (units A13 and A14)

The front section contains a number of softswitches (the softkeys beside the CRT inclusive) and rotary controls (optical switches) of which the settings are read by the microprocessor system.

The softswitches are placed in a FRONT SWITCH MATRIX which places a row of switch settings in the FRONT SWITCH BUFFER each time that the matrix is addressed by the microprocessor system. The complete matrix is scanned every 40 ms.

The optical switches generate interrupt signals IL03--LT for the microprocessor system when they are operated by the user and the microprocessor in turn addresses the circuit after which the information (from the ROTARY ENCODER) about the direction of rotation is placed on the data bus for interpretation by the microprocessor system.

The front section also contains a number of front panel leds which are controlled by the microprocessor system via LED DRIVERS.

The addresses which are generated by the microprocessor system, are decoded by a number of ADDRESS DECODERS.

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#### 6.5 CONTROL SECTION (units A5 and A6)

The control section consists mainly of a powerful MICROPROCESSOR system configuration, with an 68000 uP, a RAM MEMORY for data and a ROM MEMORY containing the system software. The MICROPROCESSOR is running at a frequency of 8 MHz which is provided by a CLOCK GENERATOR which is driven by a 16 MHz OSCILLATOR.

An ADDRESS DECODER decodes a number of addresses resulting in a number of I/O SELECT signals for the various units and a number of MEMORY SELECT signals for the various memories via the I/O and MEMORY SELECT BUFFERS.

Interrupt signals from various units are applied to an INTERRUPT PRIORITY LEVEL DECODER. From here the interrupt with the highest priority is send to the MICROPROCESSOR.

A WATCHDOG circuit detects abnormal program sequences via an OUTPUT PORT and resets the MICROPROCESSOR via the RESET/HALT block in order to restart the program. This is done by a monostable flip flop.

A BUS ARBITER controls the system bus and can give the control over the bus to processors which are fitted on options, if they ask for bus control via their BUS REQUEST signals.

The battery voltage is compared with a reference voltage by a COMPARATOR. The battery status as well as the settings of the on board SERVICE switches are applied via an INPUT PORT to the microprocessor system.

A too low battery voltage results via a SUPPLY VOLTAGE SWITCH in the saving of the memory contents.

The following functions are performed by this control section:

- Front panel settings are read and processed.
- Front panel leds are controlled.
- Time base, trigger delay counter, events counter and acquisition control logic circuits are set in accordance to the user selected settings.
- Digital processing circuits are provided with a separate program which depends on on the selected functions.
- The display system for trace, text and analog plot out data is controlled.
- If an option is installed, the complete handling is controlled.

#### 6.6 POWER SUPPLY SECTION (units A19 and A20)

The mains voltage is applied via a MAINS SWITCH + FUSE to a MAINS FILTER and to a full-wave RECTIFIER. The rectified voltage is doubled, by means of a VOLTAGE DOUBLER, if the mains voltage is below 140V. This voltage is applied to a TRANSFORMER via a FLYBACK CONVERTER. The secondary voltages are rectified by RECTIFIERS and smoothed to supply voltages for the various circuits in the instrument. These voltages are regulated by a feedback to the CONTROL + PROTECTION CIRCUIT. This circuit gives protection against over-temperature and against over- or under-voltage, For the +5 V a separate +5 V STABILIZER is fitted.

The voltages for the CRT filament and the CRT cathode are generated by an EHT converter. The cathode voltage is also multiplied in the EHT CONVERTER resulting in a high tension for the acceleration grid of the CRT.

The LINE TRIGGER CIRCUIT is not used in this instrument.

A REFERENCE VOLTAGE SOURCE circuit provides a reference voltage for internal use.

This section also contains a POWER DOWN/UP DETECTION circuit for the microprocessor. Via interrupt signal IL07--LT the microprocessor is informed about the status of the power supply.

The fan is controlled via the FAN CONTROL circuit, depending on the temperature of the oscilloscope.

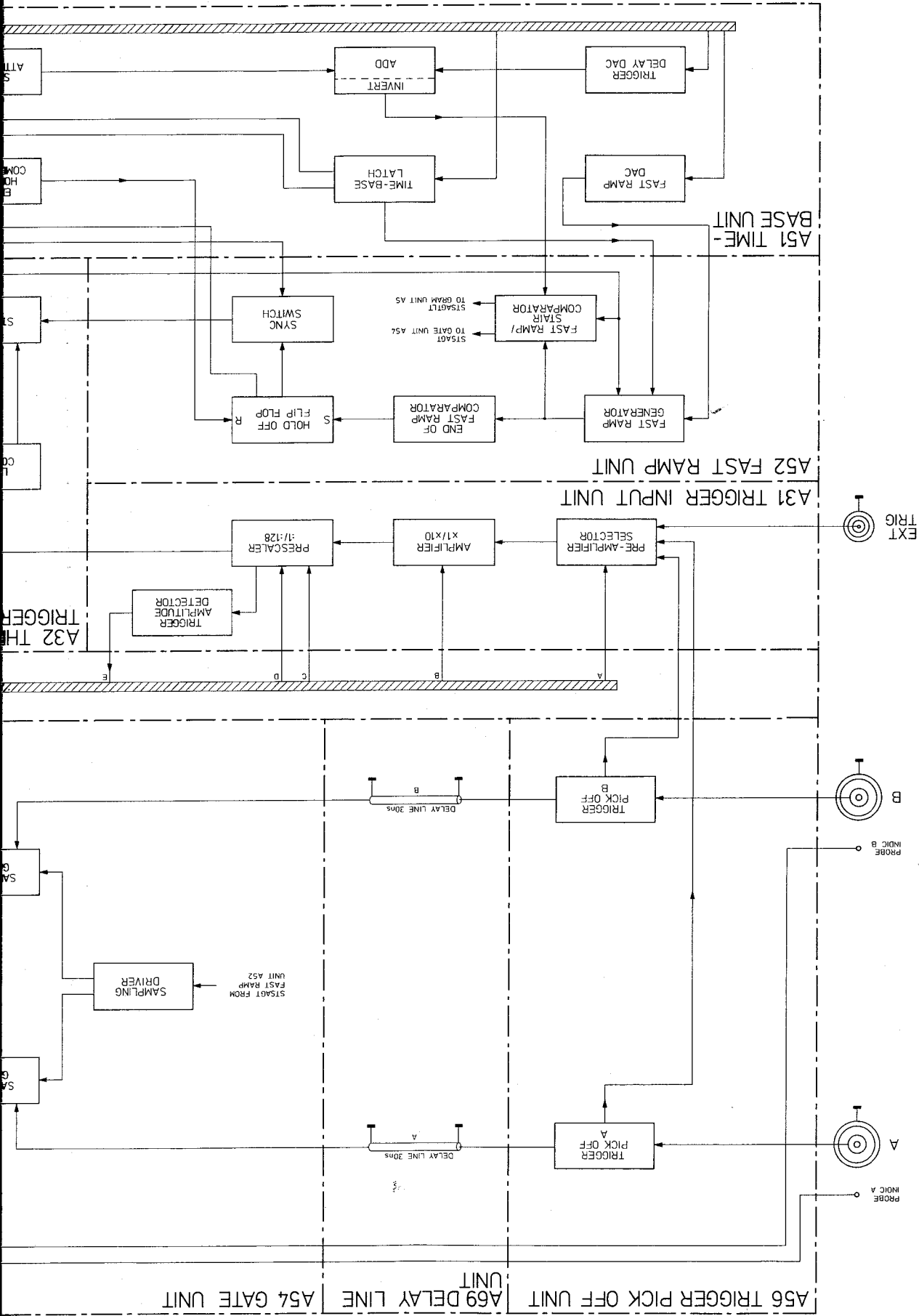
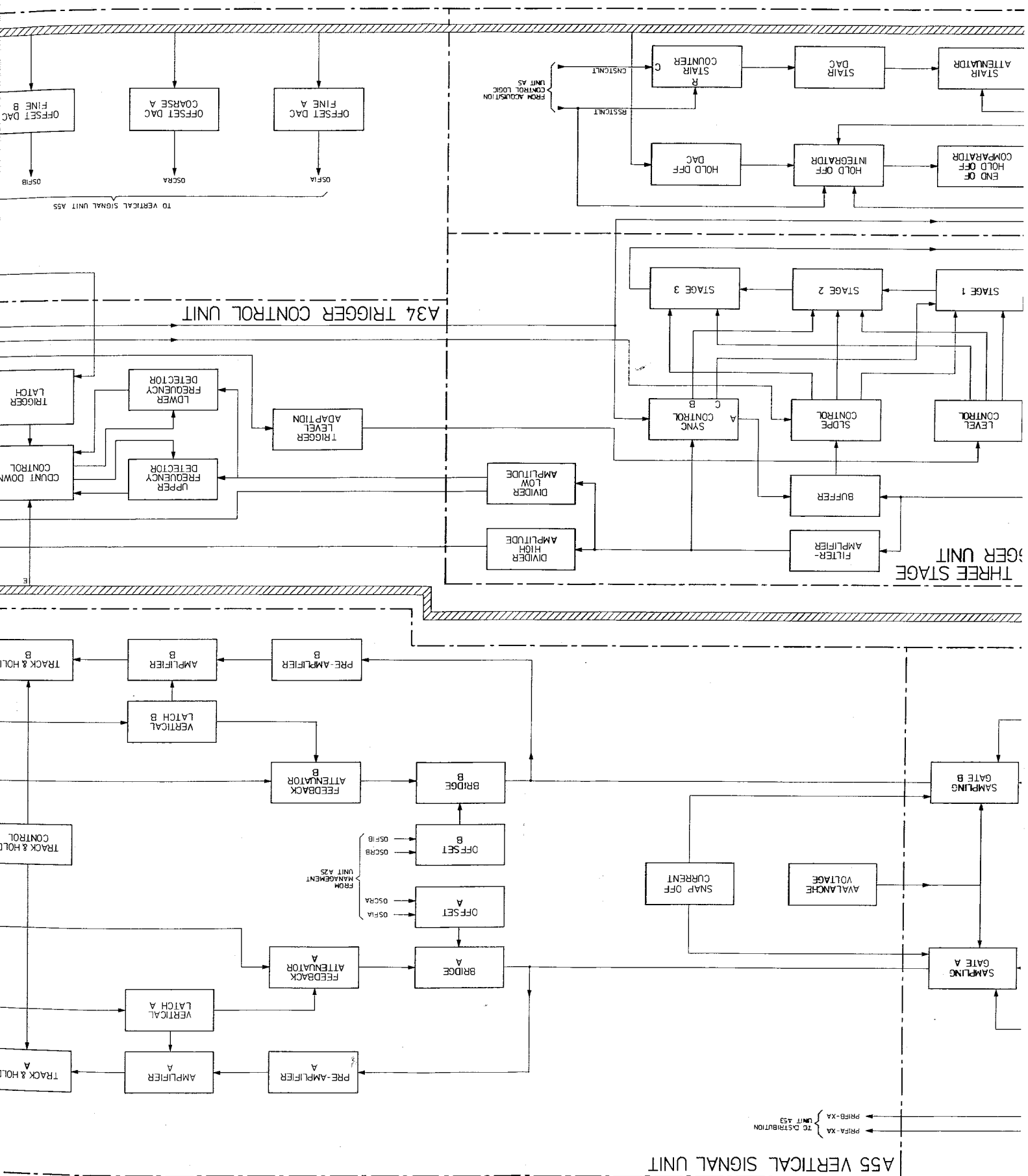
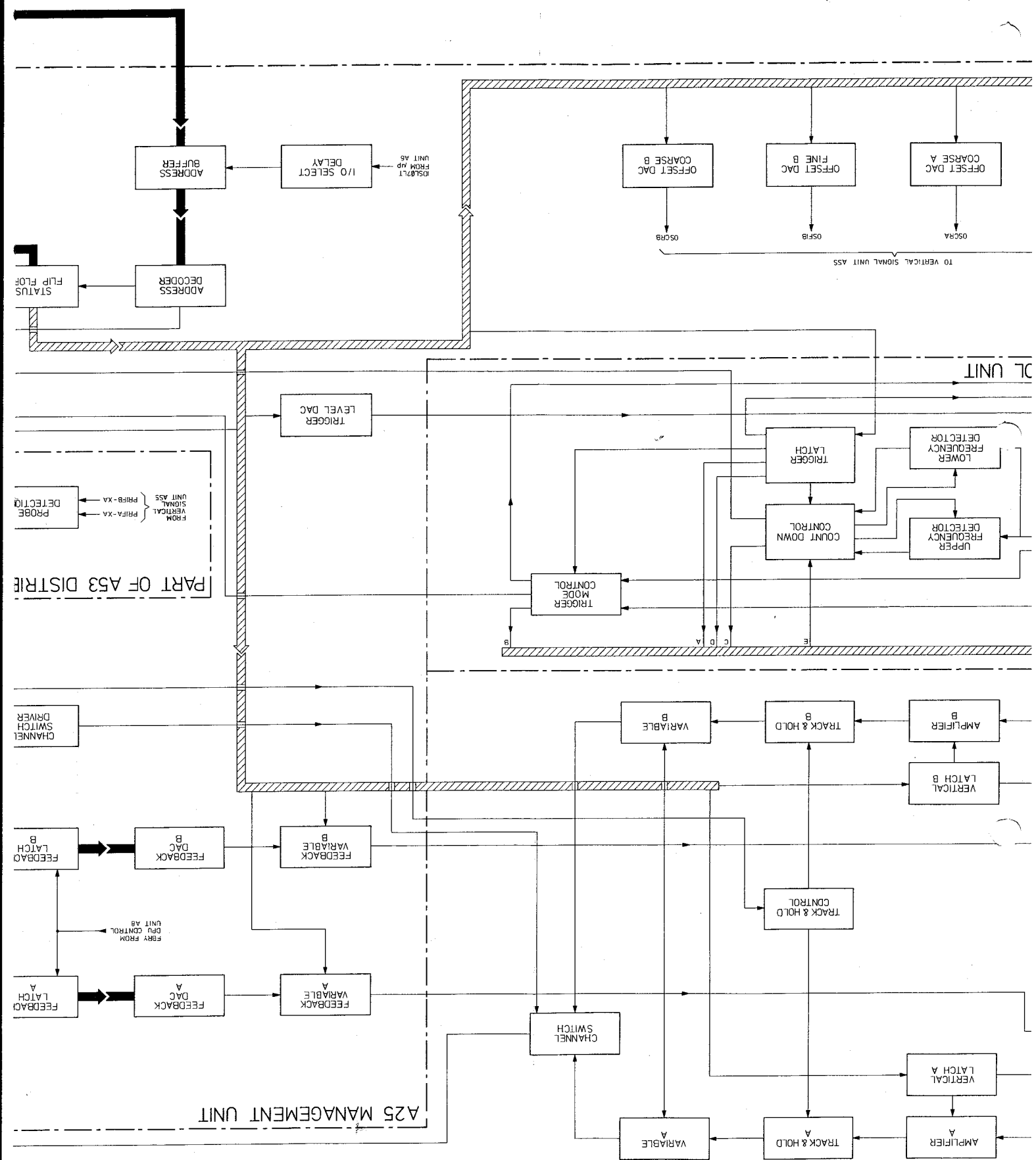
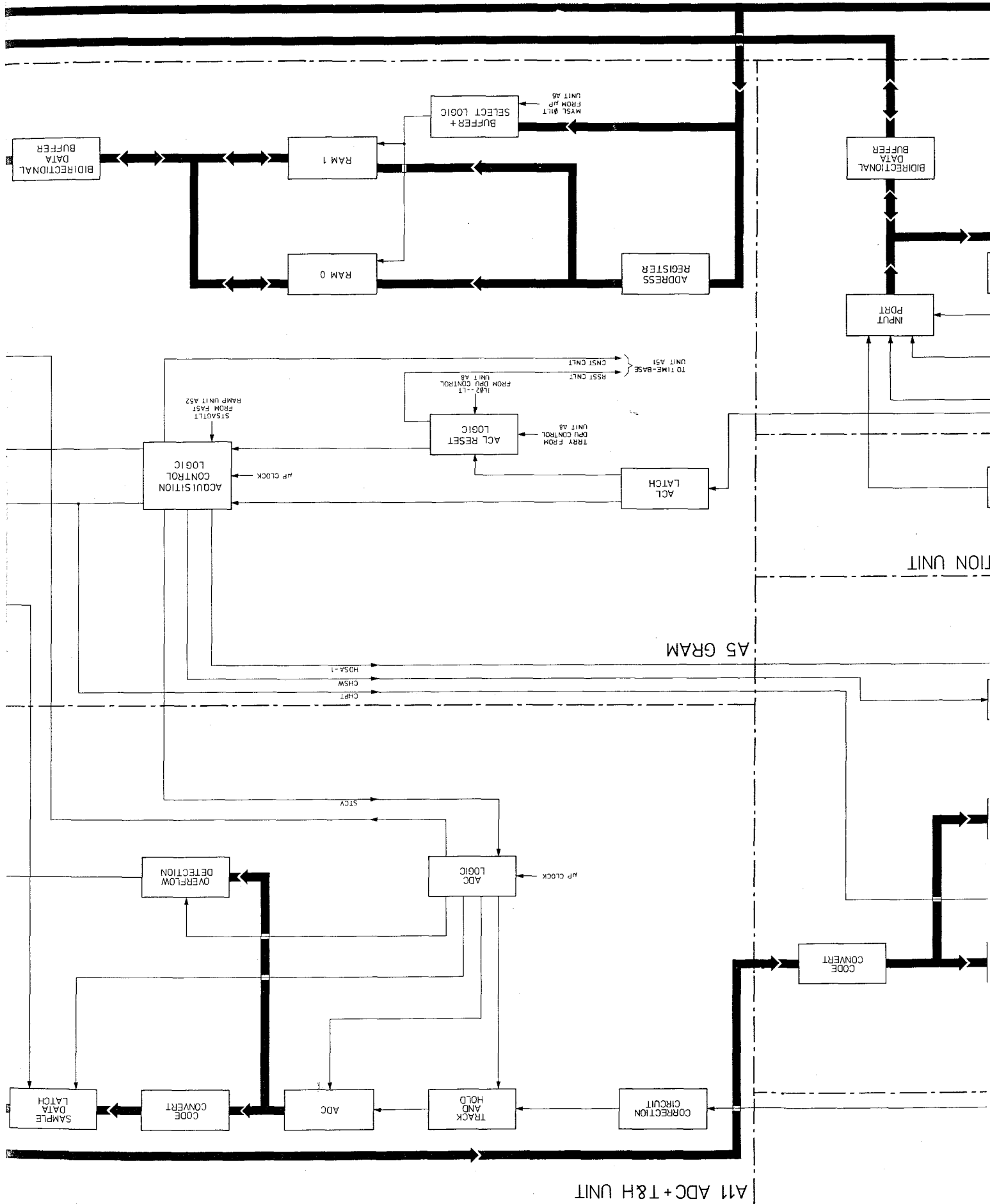
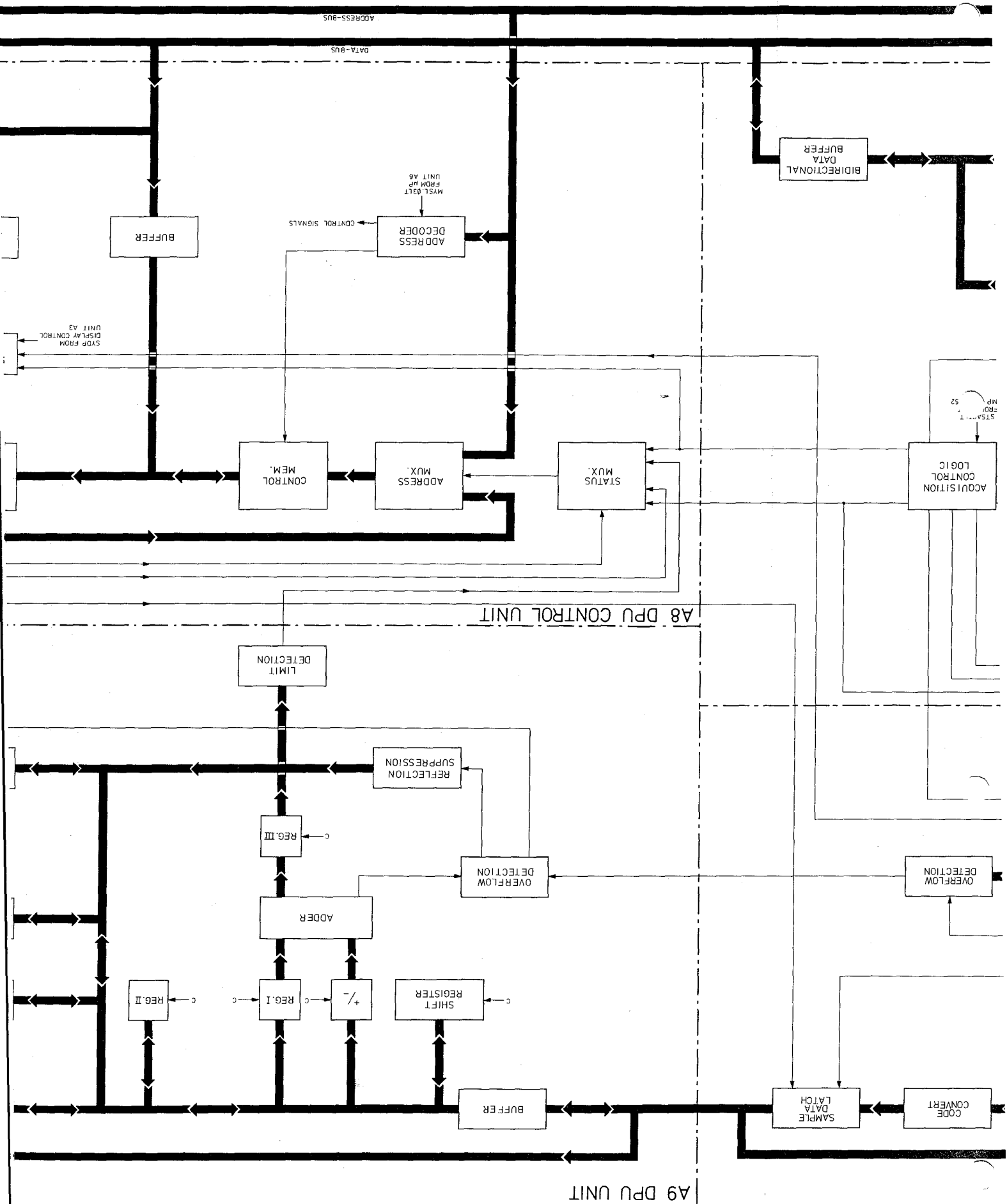


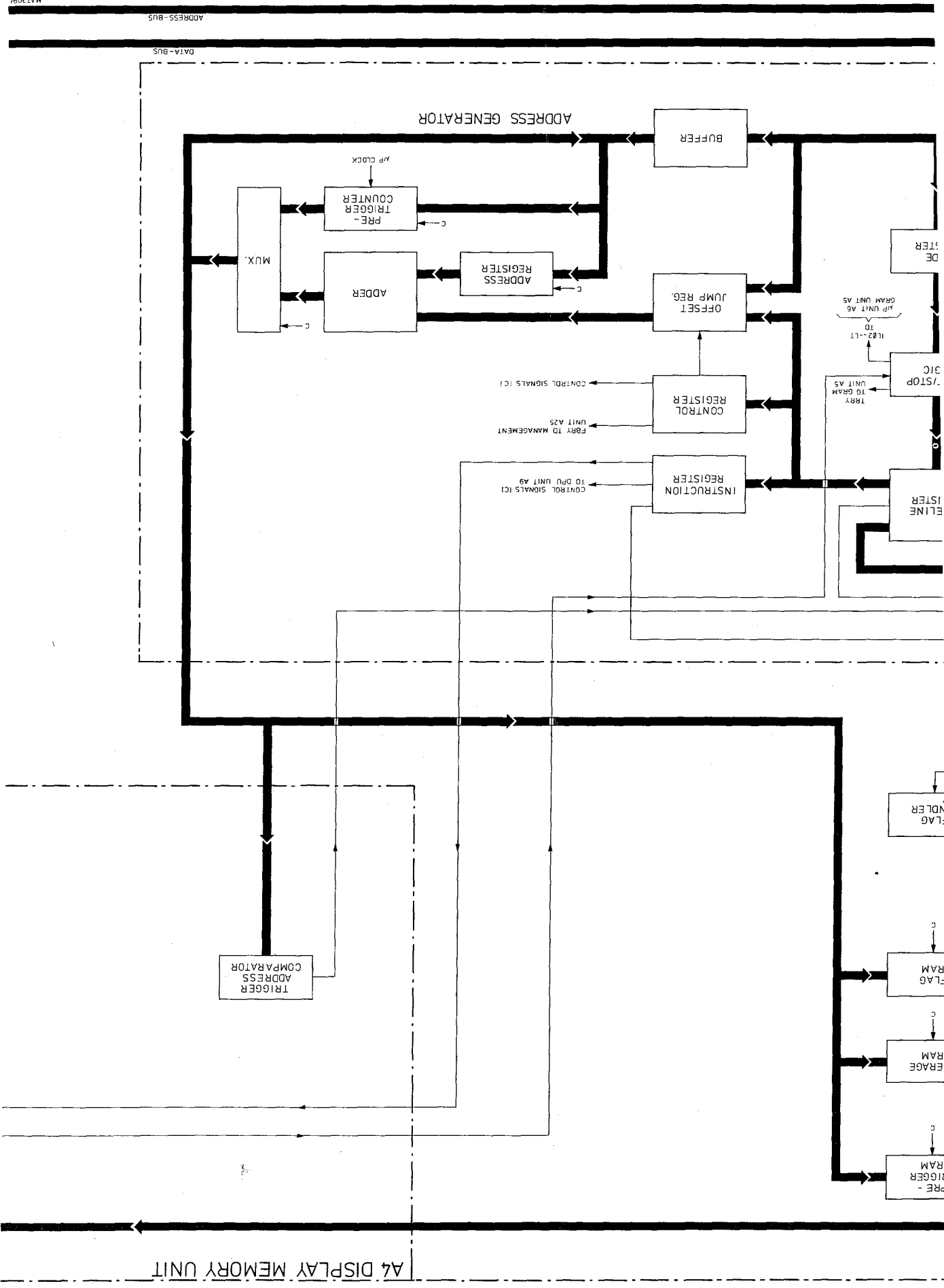
Figure 6.1 Detailed block diagram (part 1).





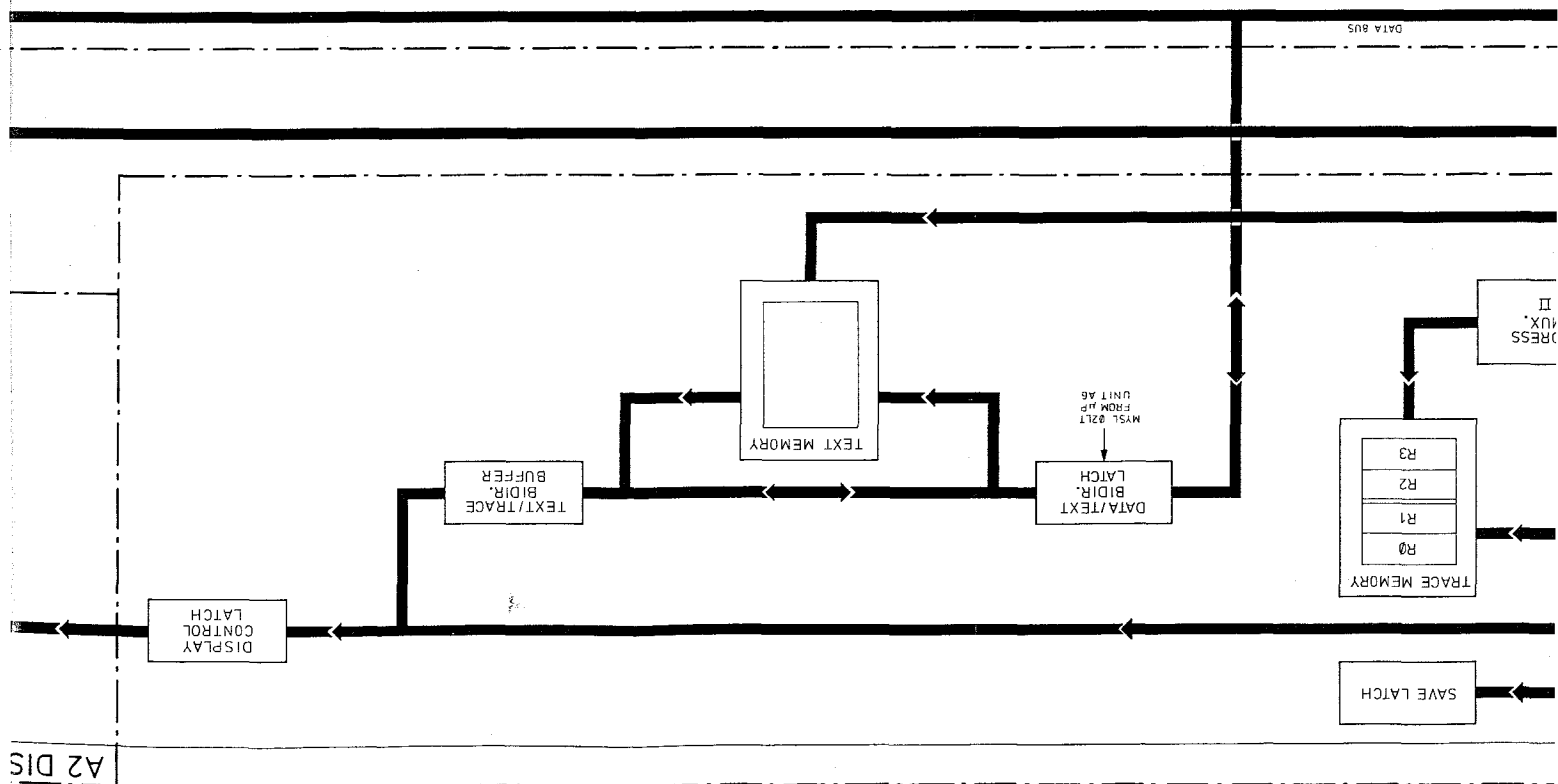
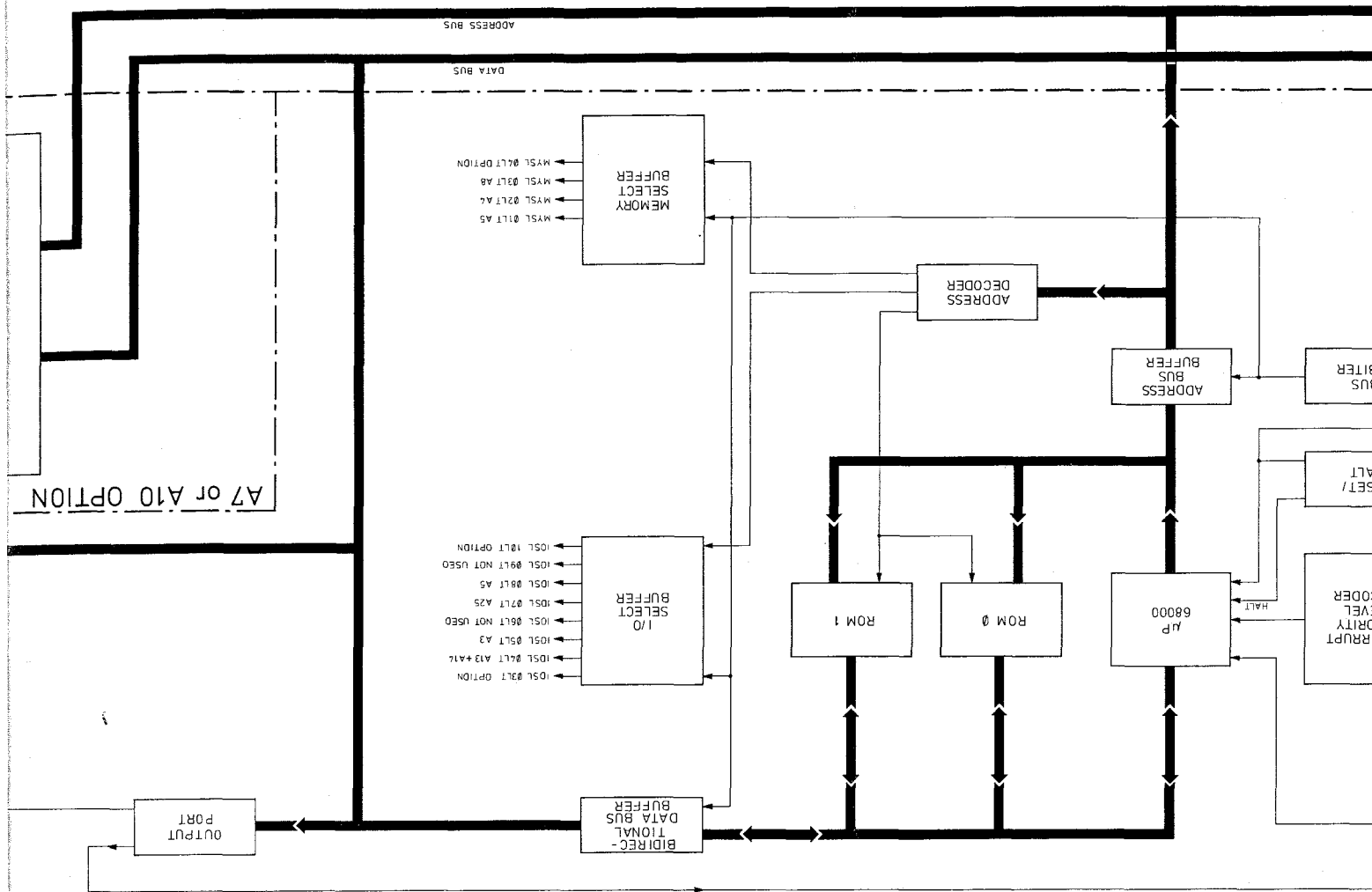


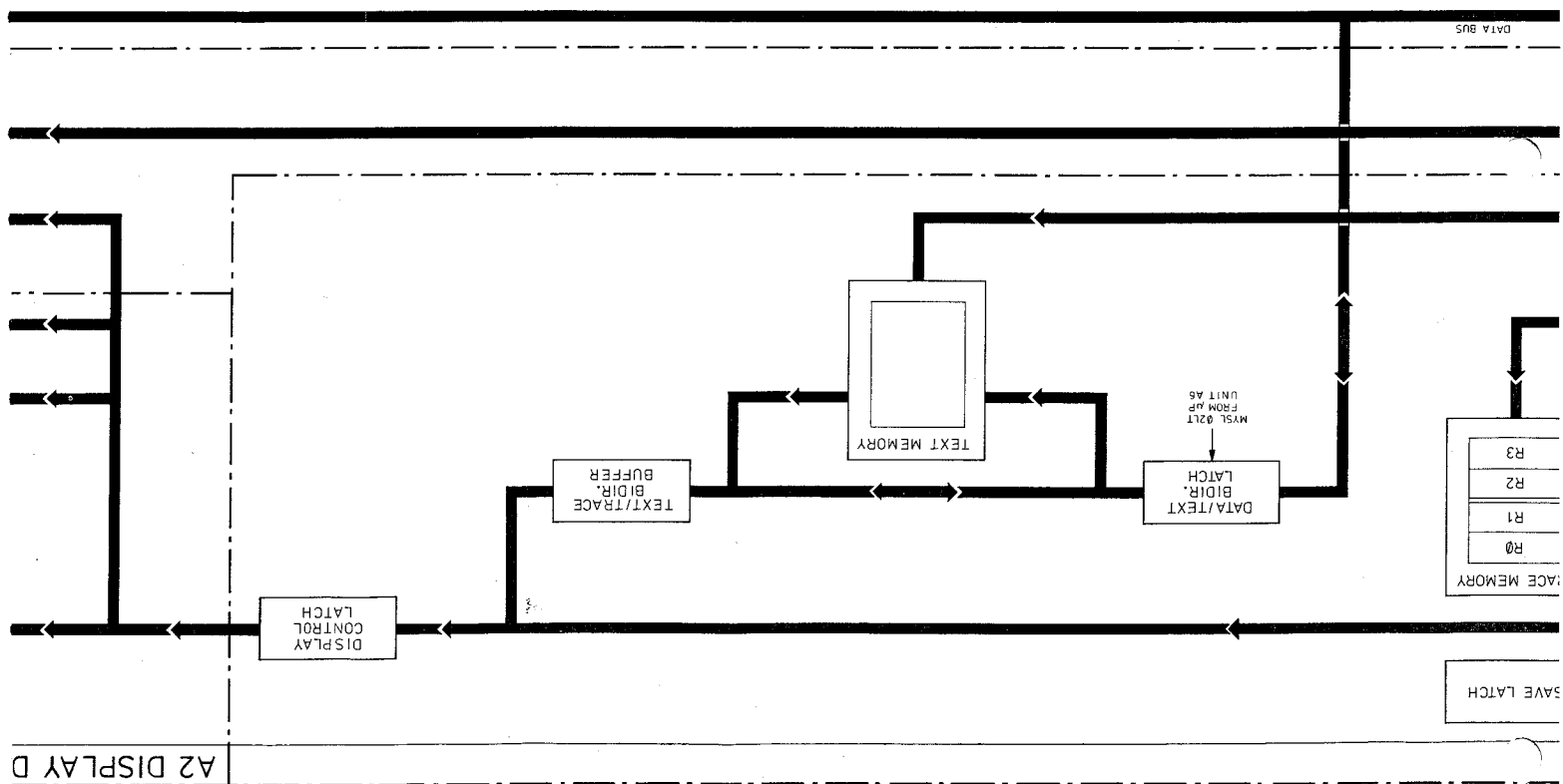
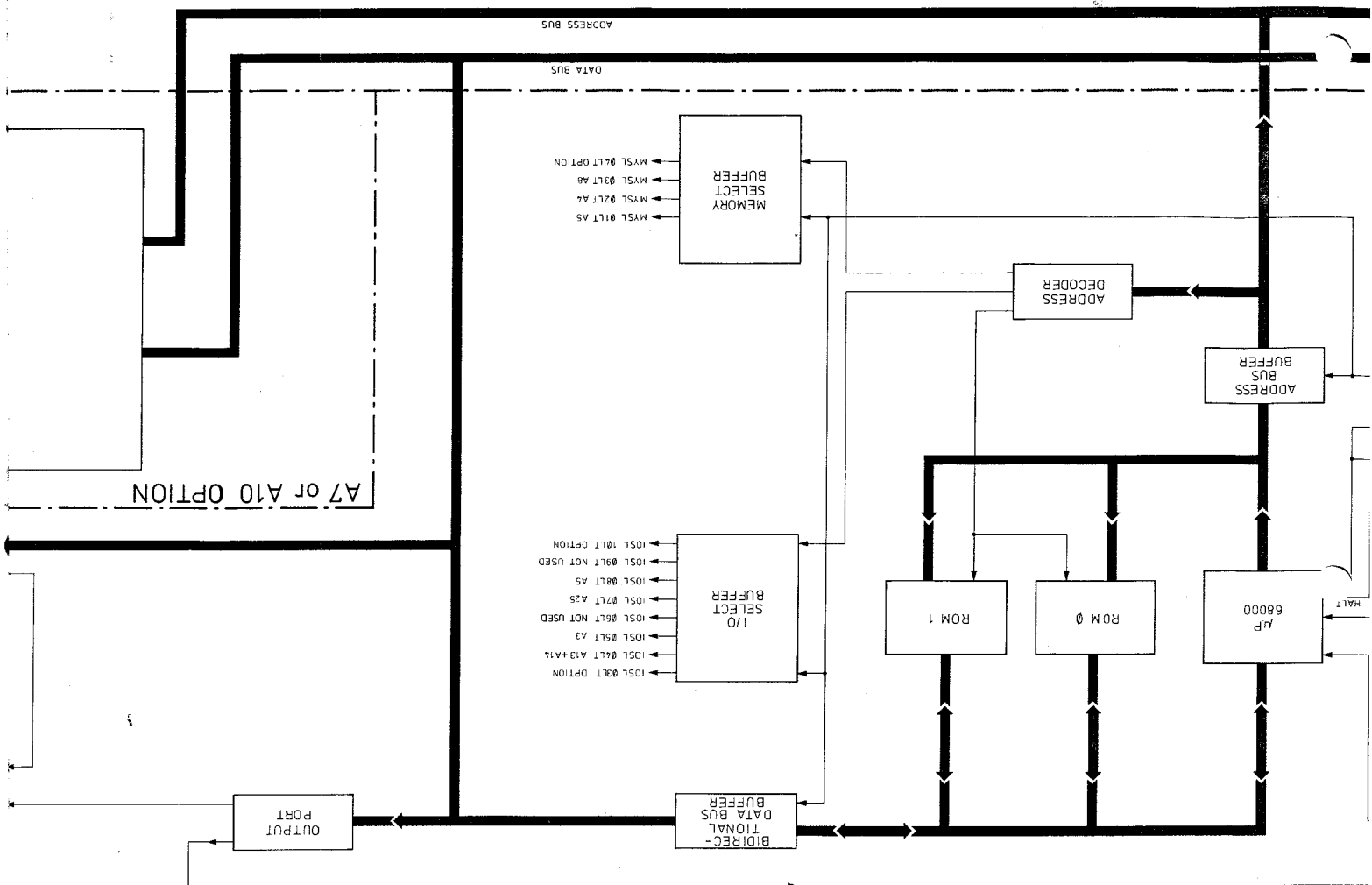


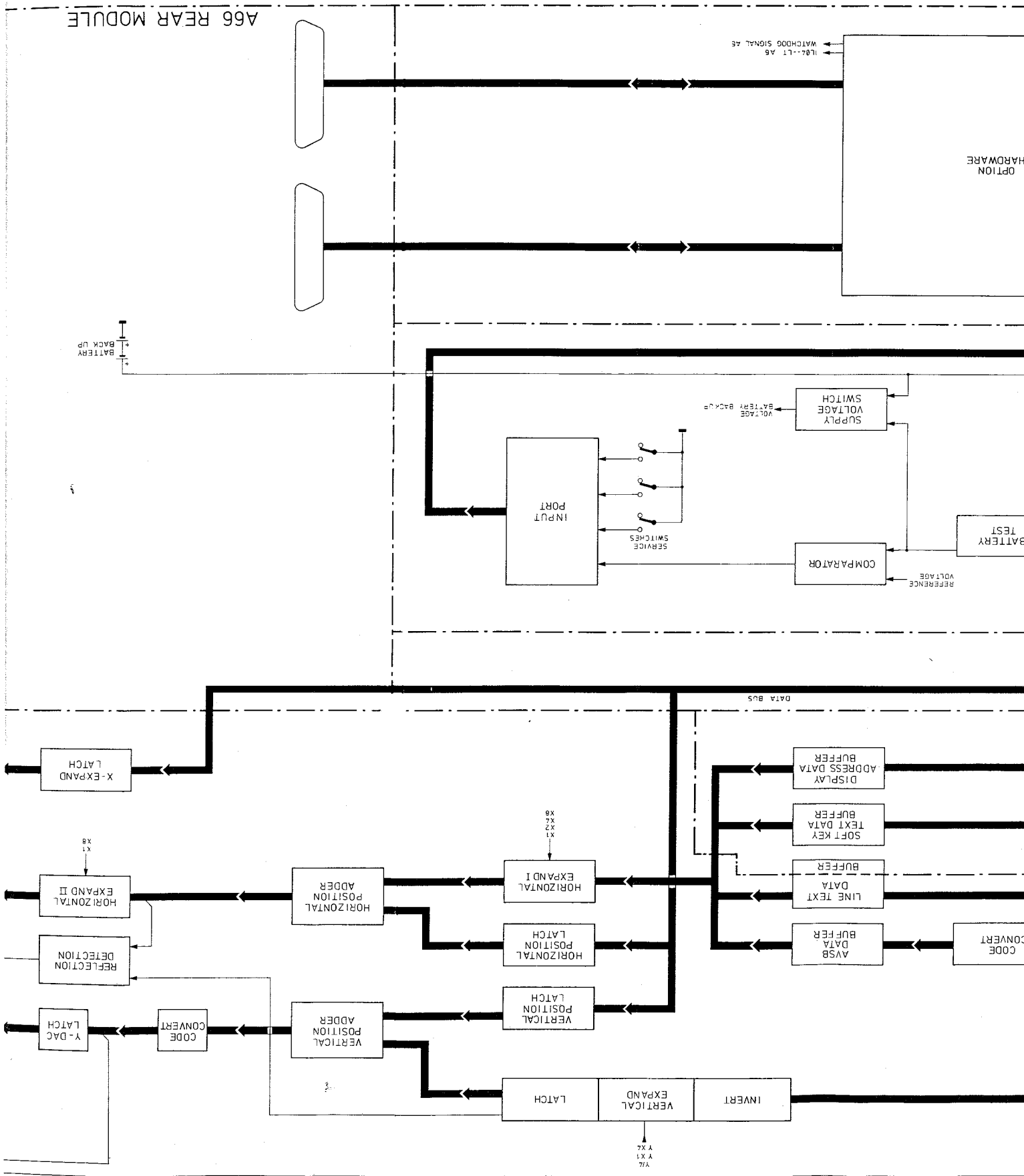


A4 DISPLAY MEMORY UNIT









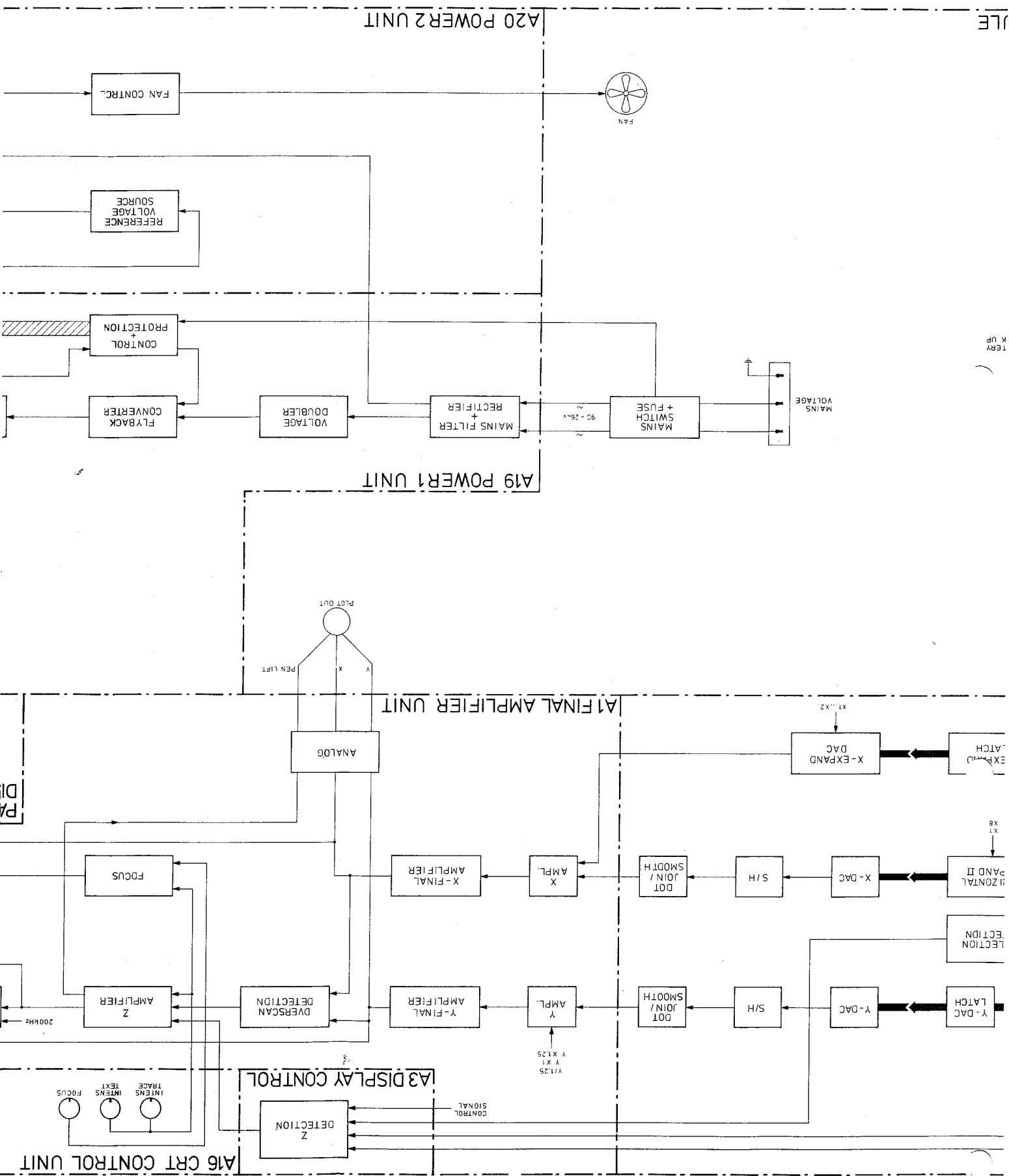
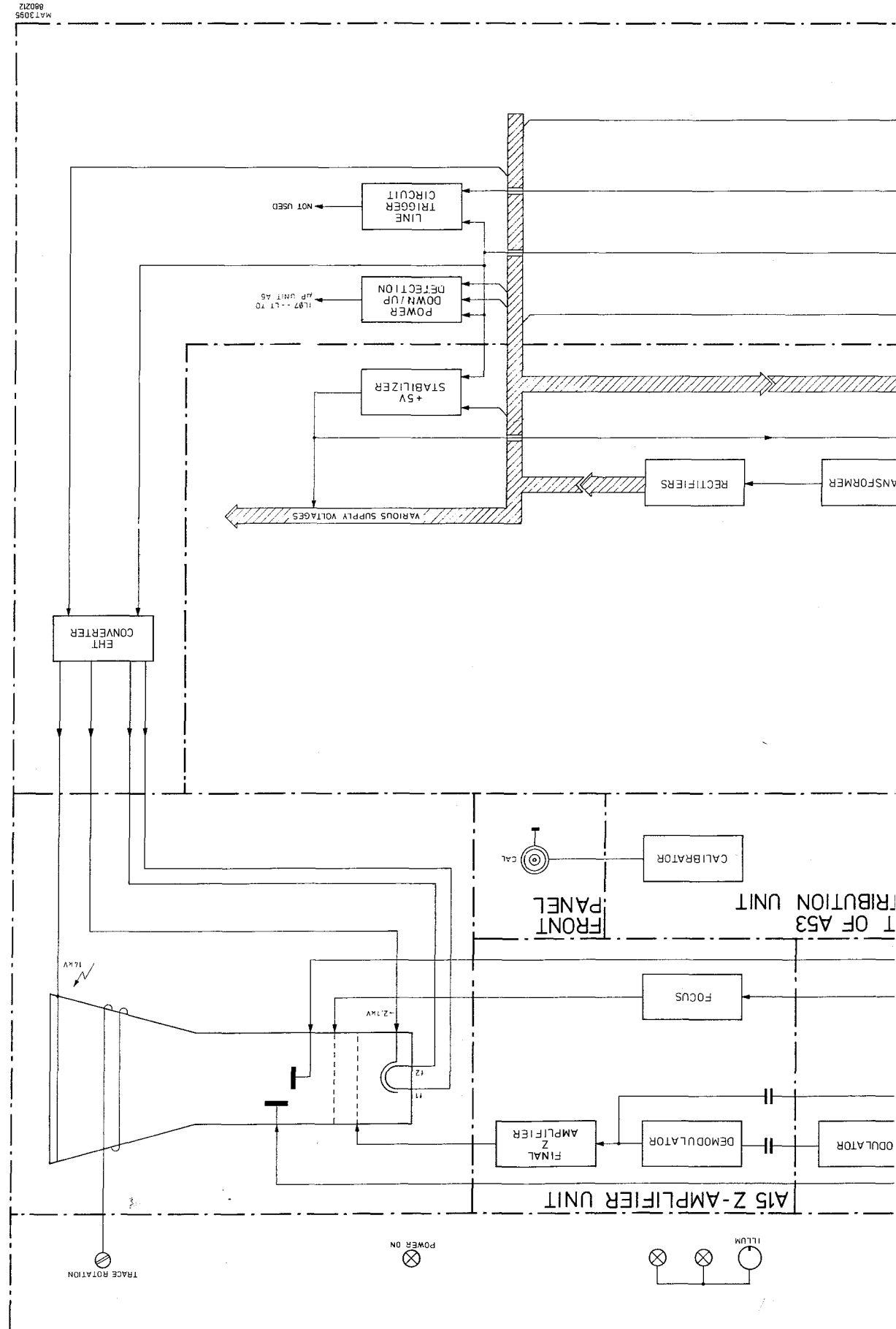


Figure 6.2 Detailed blockdiagram (part 2).



## 6.7 POWER SUPPLY AND SIGNAL DISTRIBUTION

Figure 6.3 gives a survey of how various power supply lines are distributed throughout the instrument, as well as most important signal lines.

The meaning of the signals is:

+5D	+5 Volt digital power supply lines
+V/-V	All other power supply lines
C	Control signal from or to the microprocessor
AB	Address Bus
DB	Data Bus
S	Signal
T	Trigger signal

Note that the +5D lines are supplied to the management unit A25 via a different way as the other power supply lines (+V/-V).

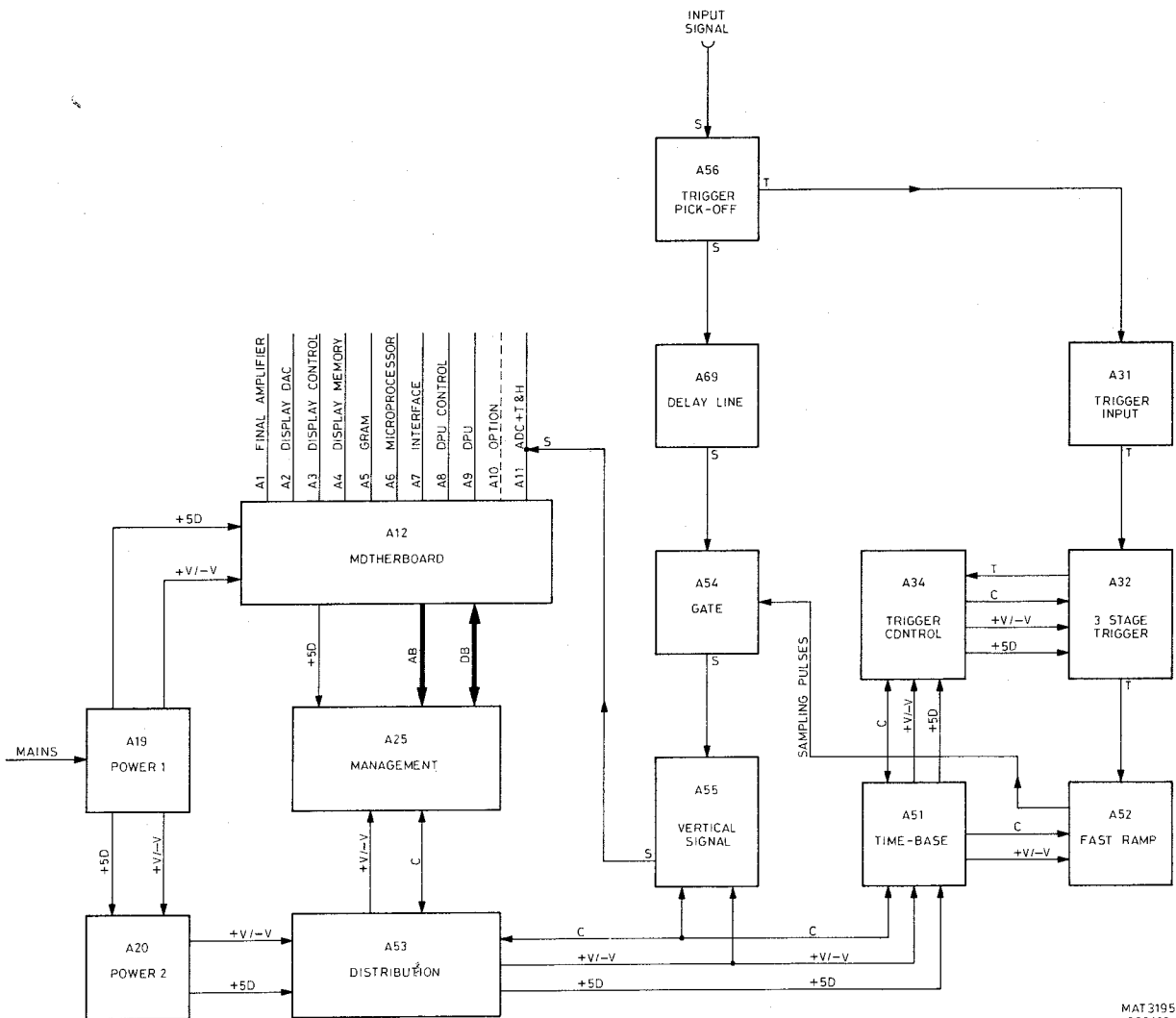


Figure 6.3 Power supply and signal distribution.