



AKAI

HOME THEATER SYSTEM

Model:
HT-A-1150

SERVICE MANUAL

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1. SAFETY PRECAUTIONS

PRECAUTIONS:

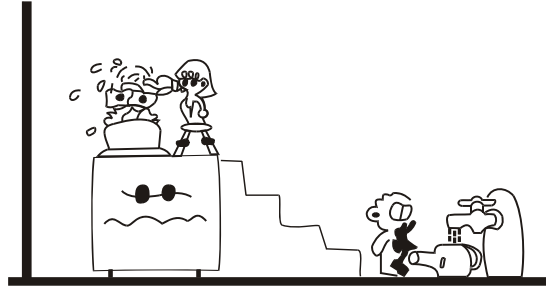
1. **Power supply:** This speaker can only use the type of power supply as specified in the instruction manual or marked on the master speaker.
2. **Power line protection:** Make sure to avoid power line being trampled, pulled or squeezed by heavy objects. In particular, be sure to hold the plug when pulling the power line from the socket. Never pull on the power line. Besides, keep the power line away from hot objects.



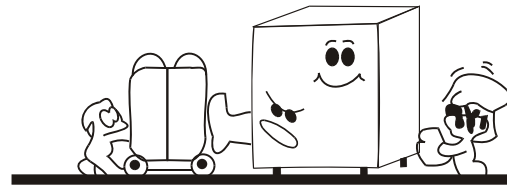
3. **Cord polarity:** The speaker cord must be correctly connected as per marking on the function panel. "+" and "-" must have correct polarity so maximize the inherent quality of the speaker. Otherwise, normal function and output will be affected.

4. **Ventilation:** This speaker has good adaptability to the environment, but pay attention to the environmental ventilation during long periods of work.

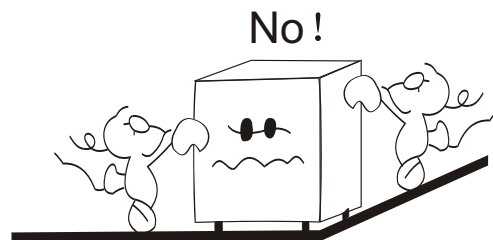
5. **Water and moisture:** Keep the sound box away from rain, water spray, water splash and wet environment, such as bath, kitchen, water basin, washing basin, damp basement, swimming pool, etc.



6. **Removing cabinet:** In case of speaker failure or problems due to improper use, don't dismantle the unit to repair or check by yourself. Please turn off the power and use after checked by specialists to avoid causing personal accident.



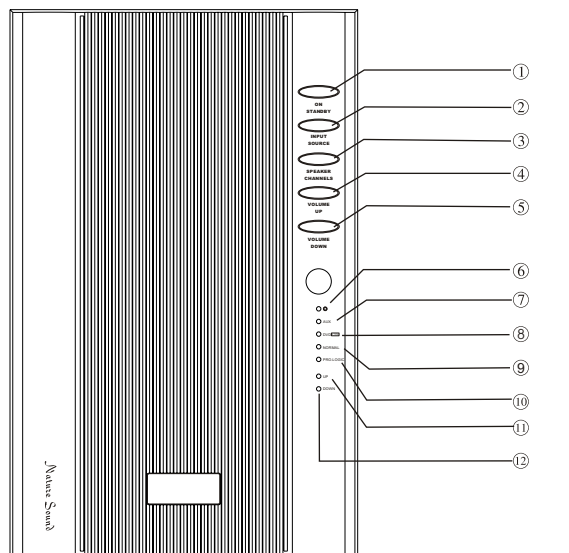
7. **Appearance cleaning:** Don't use volatile solutions to clean the speaker to avoid damaging the appearance.



8. **Please cut off the power:** If you don't use the sound system for a long time, please remove the cable wire or disconnect the power to ensure the speaker safety and household safety.

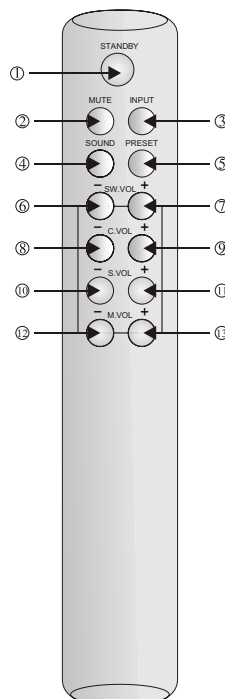
2. LOCATION OF USERS CONTROLS

FRONT PANEL INSTRUCTION :



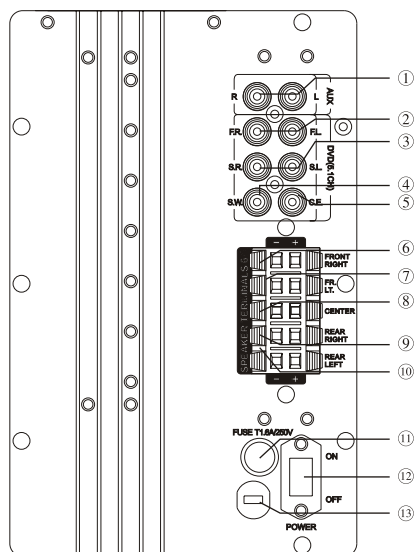
- | | | | |
|---------------------|---|------------------------------|---------------------------------------|
| ON
STANDBY | ① Power switch button(standby) switch on or off for waiting or on condition | INPUT
SOURCE | ② Signal input selection |
| SPEAKER
CHANNELS | ③ Sound field selection | VOLUME
UP | ④ Master volume in increase selection |
| VOLUME
DOWN | ⑤ Master volume decrease selection | ⑥ Working /standby indicator | |
| AUX | ⑦ AUX signal input indicator | DVD
PLAY | ⑧ DVD signal input indicator |
| NORMAL | ⑨ NORMAL sound field indicator | PRO LOGIC | ⑩ Pro.logic sound field indicator |
| UP | ⑪ Volume increase indicator | DOWN | ⑫ Volume decrease indicator |

REMOTE CONTROL INSTRUCTION :



- | | |
|---|----------------------|
| ① | Working/stanby |
| ② | mute button |
| ③ | input signal button |
| ④ | Sound field select |
| ⑤ | preset button |
| ⑥ | bass volume down |
| ⑦ | bass volume up |
| ⑧ | center volume down |
| ⑨ | center volume up |
| ⑩ | surround volume down |
| ⑪ | surround volume up |
| ⑫ | main volume down |
| ⑬ | main volume up |

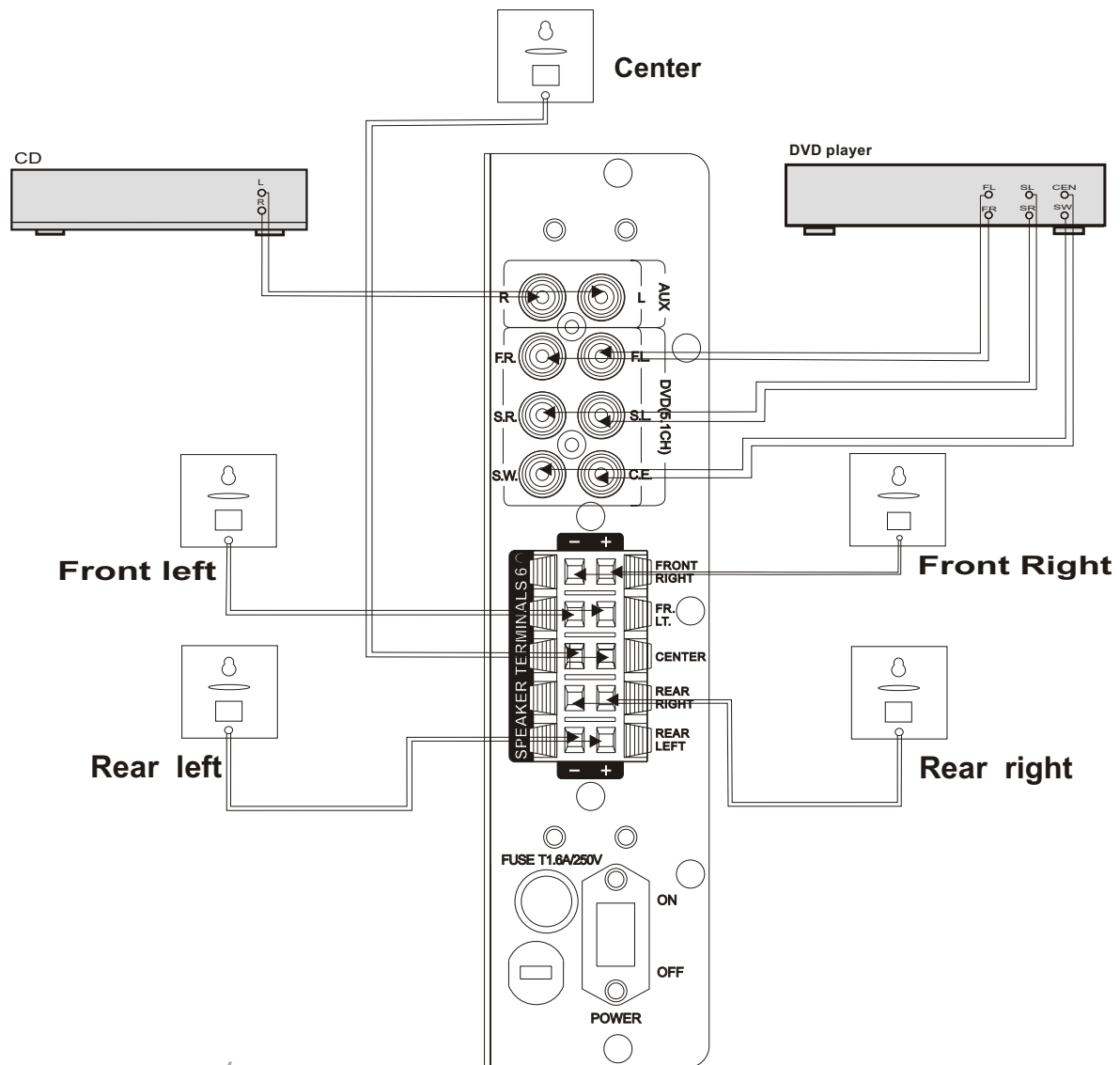
BACK PANEL DESCRIPTION:



- | | |
|-----------------------|-----------------------|
| ① AUX L/R INPUT | ② DVD F.R./FL.INPUT |
| ③ DVD S.R./S.L.INPUT | ④ DVD S.W.INPUT |
| ⑤ DVD C.E.INPUT | ⑥ SPEAKER OUTPUT F.R. |
| ⑦ SPEAKER OUTPUT F.L. | ⑧ SPEAKER OUTPUT C.E. |
| ⑨ SPEAKER OUTPUT S.R. | ⑩ SPEAKER OUTPUT S.L. |
| ⑪ FUSE T1.6A/250V | ⑫ POWER SWITCH |
| ⑬ POWER | |

3. CONNECTING TO EQUIPMENT

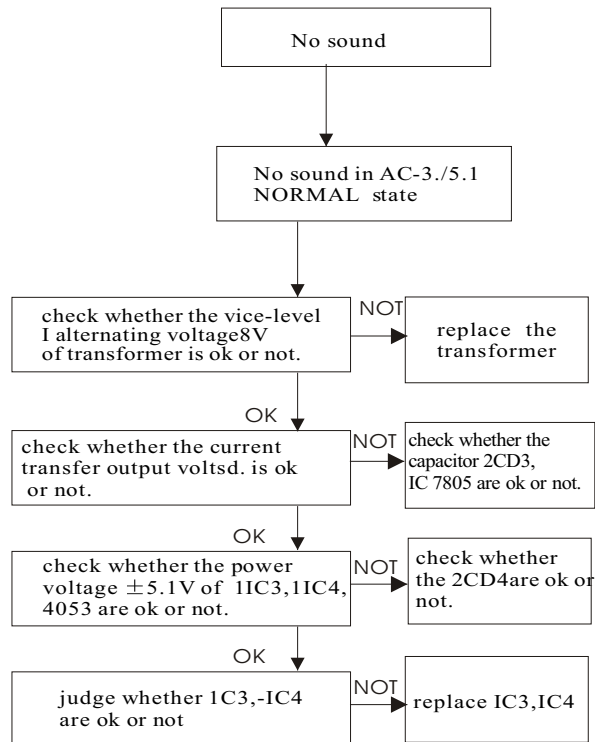
SYSTEM CONNECTION:



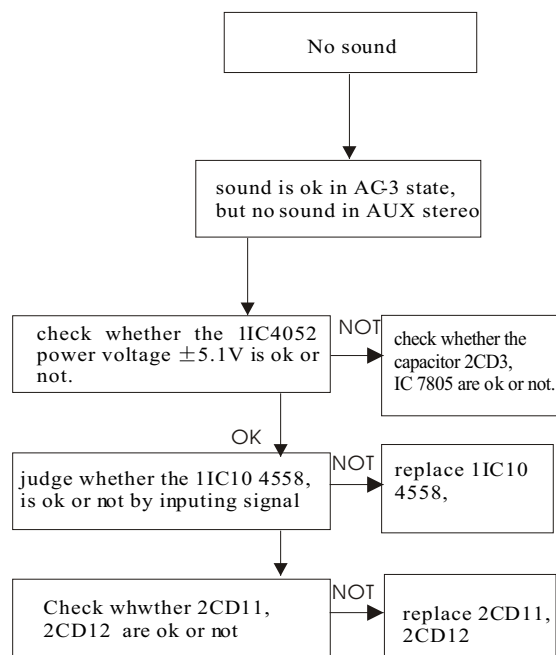
4. TROUBLESHOOTING GUIDE

TROUBLE SHOOTING AND RESOLUTION

1

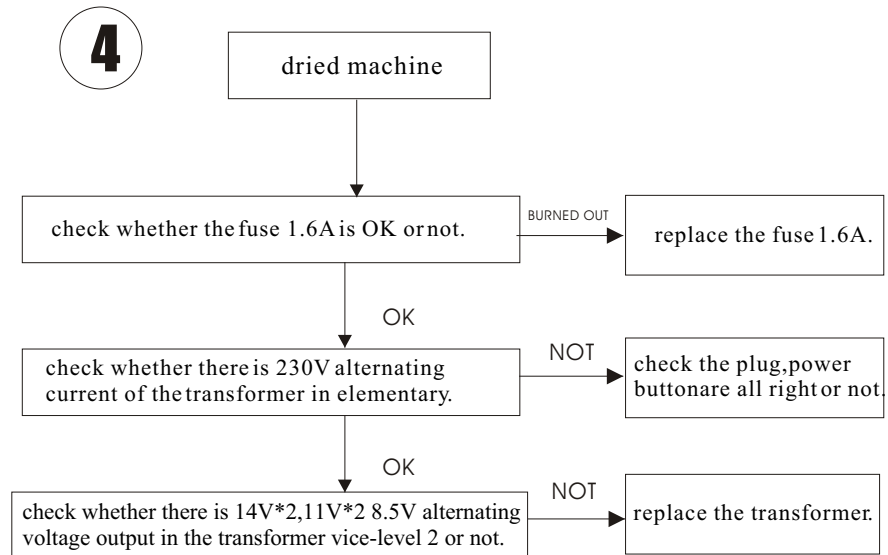


2



4. TROUBLESHOOTING GUIDE

TROUBLE SHOOTING AND RESOLUTION



5

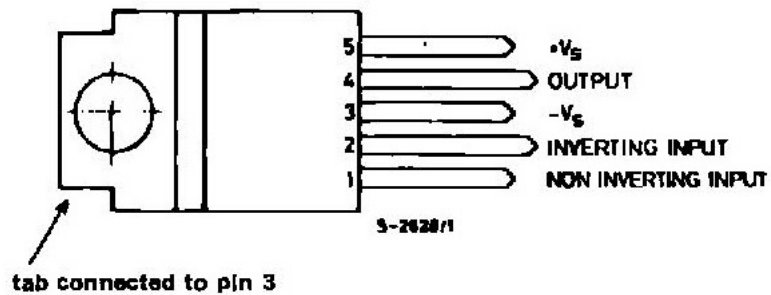
Error	Possible reason	Obivating
No sound	The power plug is not exactly inserted. The connection of output and input is not well The input format is not right The volume control be settled in the minimum Rest estate	Insert the plug in right place Connect the output and input cables Adjust the volume

5. INTERNAL BLOCK DIAGRAM OF ICS

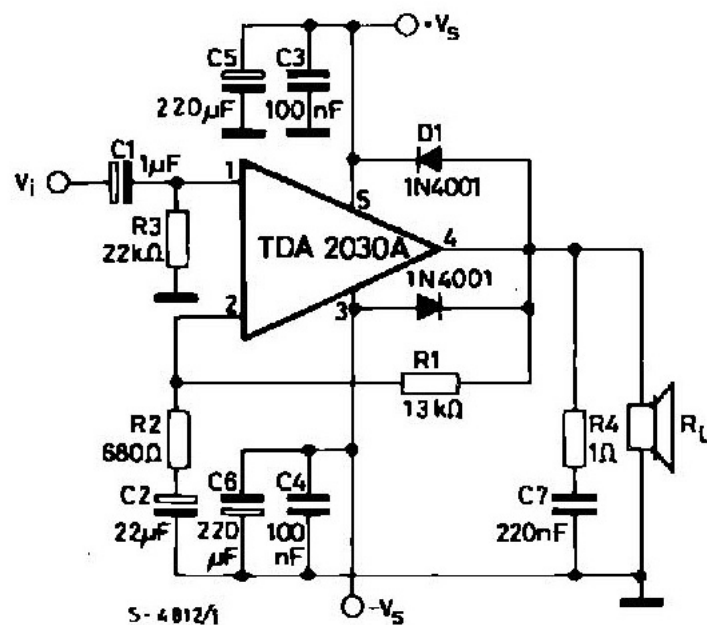
TDA2030A

TDA2030A

PIN CONNECTION (Top view)



TEST CIRCUIT



5. INTERNAL BLOCK DIAGRAM OF ICS

TDA2030A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 22	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 15	V
I_o	Peak Output Current (internally limited)	3.5	A
P_{tot}	Total Power Dissipation at $T_{case} = 90^\circ\text{C}$	20	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to $+150$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

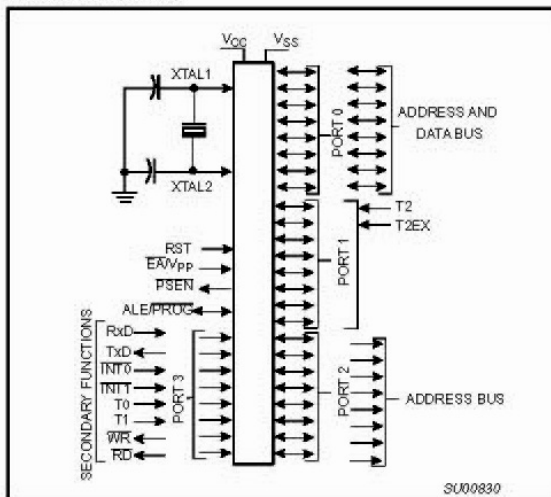
(Refer to the test circuit, $V_s = \pm 16\text{V}$, $T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 22	V
I_d	Quiescent Drain Current			50	80	mA
I_b	Input Bias Current	$V_s = \pm 22\text{V}$		0.2	2	μA
V_{os}	Input Offset Voltage	$V_s = \pm 22\text{V}$		± 2	± 20	mV
I_{os}	Input Offset Current			± 20	± 200	nA
P_O	Output Power	$d = 0.5\%$, $G_v = 26\text{dB}$ $f = 40$ to 15000Hz $R_L = 4\Omega$ $R_L = 8\Omega$ $V_s = \pm 19\text{V}$ $R_L = 8\Omega$	15 10 13	18 12 16		W
BW	Power Bandwidth	$P_O = 15\text{W}$ $R_L = 4\Omega$		100		kHz
SR	Slew Rate			8		V/ μsec
G_v	Open Loop Voltage Gain	$f = 1\text{kHz}$		80		dB
G_v	Closed Loop Voltage Gain	$f = 1\text{kHz}$	25.5	26	26.5	dB
d	Total Harmonic Distortion	$P_O = 0.1$ to 14W $R_L = 4\Omega$ $f = 40$ to 15000Hz $f = 1\text{kHz}$ $P_O = 0.1$ to 9W , $f = 40$ to 15000Hz $R_L = 8\Omega$		0.08 0.03 0.5		% % %
d_2	Second Order CCIF Intermodulation Distortion	$P_O = 4\text{W}$, $f_2 - f_1 = 1\text{kHz}$, $R_L = 4\Omega$		0.03		%
d_3	Third Order CCIF Intermodulation Distortion	$f_1 = 14\text{kHz}$, $f_2 = 15\text{kHz}$ $2f_1 - f_2 = 13\text{kHz}$		0.08		%
e_N	Input Noise Voltage	B = Curve A B = 22Hz to 22kHz		2 3	10	μV μV
i_N	Input Noise Current	B = Curve A B = 22Hz to 22kHz		50 80	200	pA pA
S/N	Signal to Noise Ratio	$R_L = 4\Omega$, $R_g = 10\text{k}\Omega$, B = Curve A $P_O = 15\text{W}$ $P_O = 1\text{W}$		106 94		dB dB
R_i	Input Resistance (pin 1)	(open loop) $f = 1\text{kHz}$	0.5	5		M Ω
SVR	Supply Voltage Rejection	$R_L = 4\Omega$, $R_g = 22\text{k}\Omega$ $G_v = 26\text{dB}$, $f = 100\text{Hz}$		54		dB
T_j	Thermal Shut-down Junction Temperature			145		$^\circ\text{C}$

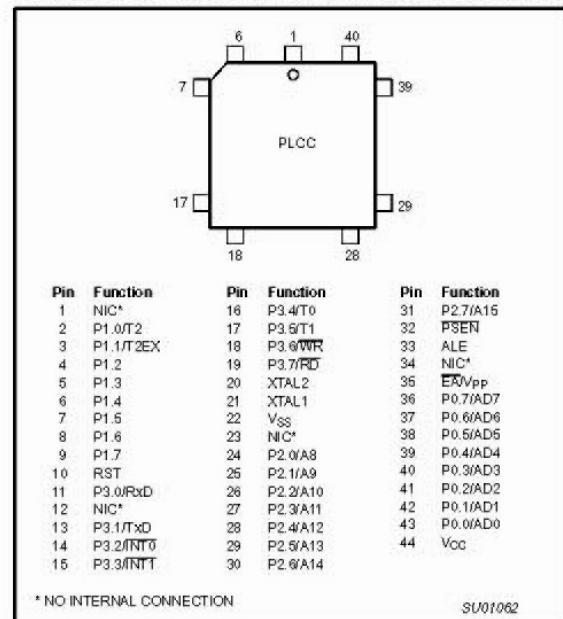
5. INTERNAL BLOCK DIAGRAM OF ICS

89C52

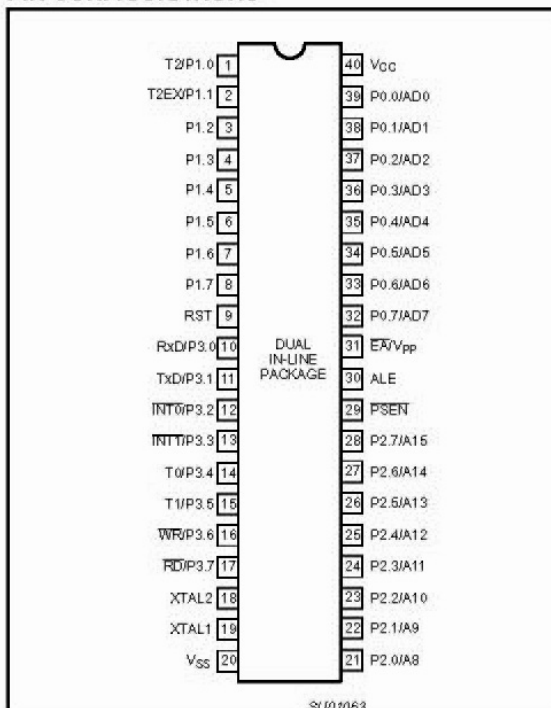
LOGIC SYMBOL



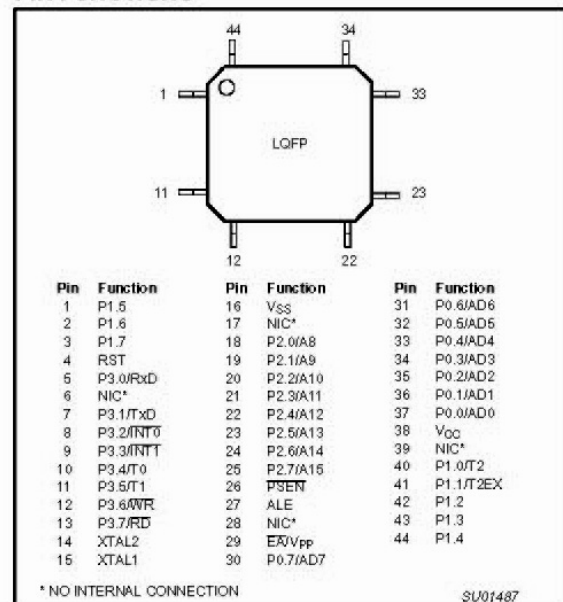
PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



PLASTIC DUAL IN-LINE PACKAGE PIN CONFIGURATIONS



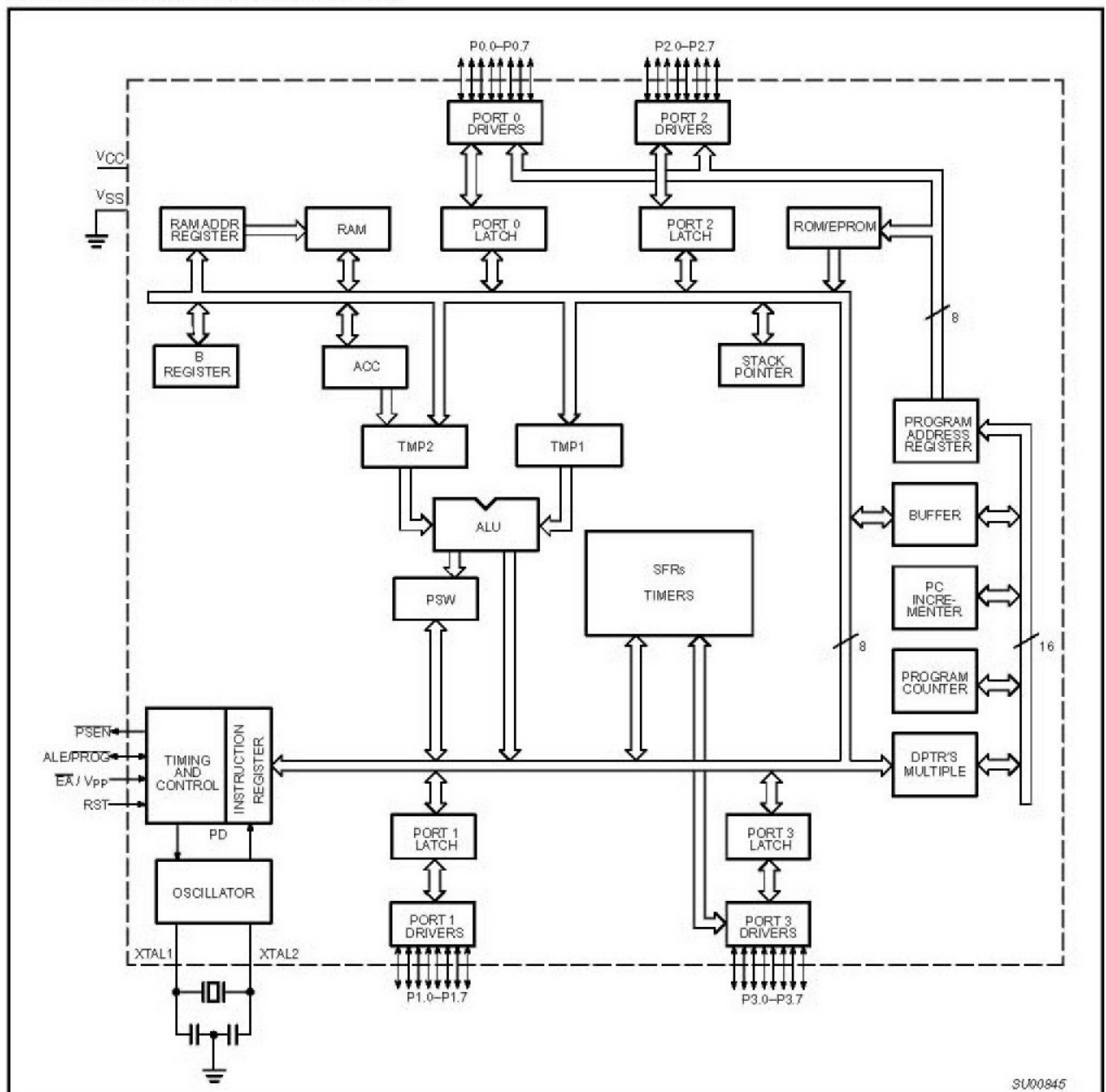
LOW PROFILE QUAD FLAT PACK PIN FUNCTIONS



5. INTERNAL BLOCK DIAGRAM OF ICS

89C52

BLOCK DIAGRAM 2 (CPU-ORIENTED)



5. INTERNAL BLOCK DIAGRAM OF ICS

89C52

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	PLCC	LQFP		
V _{SS}	20	22	16	I	Ground: 0 V reference.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	39–32	43–36	37–30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during Flash programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include: T2 (P1.0): Timer/Counter 2 external count input/clockout (see Programmable Clock-Out) T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	1 2 21–28	2 3 24–31	40 41 18–25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during Flash programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below: RxD (P3.0): Serial input port TxD (P3.1): Serial output port INT0 (P3.2): External interrupt INT1 (P3.3): External interrupt T0 (P3.4): Timer 0 external input T1 (P3.5): Timer 1 external input WR (P3.6): External data memory write strobe RD (P3.7): External data memory read strobe
RST	17 9	19 10	13 4	O	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	33	27	O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (12-clk) or 1/3 (6-clk Mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during Flash programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.
PSEN	29	32	26	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/V _{pp}	31	35	29	I	External Access Enable/Programming Supply Voltage: EA must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFFH/1FFFFH/3FFFFH/7FFFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than the on-chip Flash. This pin also receives the 5 V / 12 V programming supply voltage (V _{pp}) during Flash programming. If security bit 1 is programmed, EA will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5 V or V_{SS} – 0.5 V, respectively.

5. INTERNAL BLOCK DIAGRAM OF ICS

CD4053B

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V_{p-p} can be achieved by digital signal amplitudes of 4.5V to 20V (if $V_{DD}-V_{SS} = 3V$, a $V_{DD}-V_{EE}$ of up to 13V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13V, a $V_{DD}-V_{SS}$ of at least 4.5V is required). For example, if $V_{DD} = +4.5V$, $V_{SS} = 0V$, and $V_{EE} = -13.5V$, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic 0 is present at the inhibit input $\bar{I}$, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the $\bar{O}$ CHANNEL IN/OUT $\bar{O}$ terminals are the outputs and the $\bar{O}$ COMMON OUT/ $\bar{I}$ $\bar{O}$ terminals are the inputs.

Features

- ¥ Wide Range of Digital and Analog Signal Levels
 - Digital 3V to 20V
 - Analog $\leq 20V_{p-p}$
- ¥ Low ON Resistance, 125 Ω (Typ) Over 15V_{p-p} Signal Input Range for $V_{DD}-V_{EE} = 18V$
- ¥ High OFF Resistance, Channel Leakage of $\pm 100pA$ (Typ) at $V_{DD}-V_{EE} = 18V$
- ¥ Logic-Level Conversion for Digital Addressing Signals of 3V to 20V ($V_{DD}-V_{SS} = 3V$ to 20V) to Switch Analog Signals to 20V_{p-p} ($V_{DD}-V_{EE} = 20V$)
- ¥ Matched Switch Characteristics, $r_{ON} = 5\Omega$ (Typ) for $V_{DD}-V_{EE} = 15V$
- ¥ Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 μW (Typ) at $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V$
- ¥ Binary Address Decoding on Chip
- ¥ 5V, 10V and 15V Parametric Ratings
- ¥ 10% Tested for Quiescent Current at 20V
- ¥ Maximum Input Current of 1 μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C
- ¥ Break-Before-Make Switching Eliminates Channel Overlap

Applications

- ¥ Analog and Digital Multiplexing and Demultiplexing
- ¥ A/D and D/A Conversion
- ¥ Signal Gating

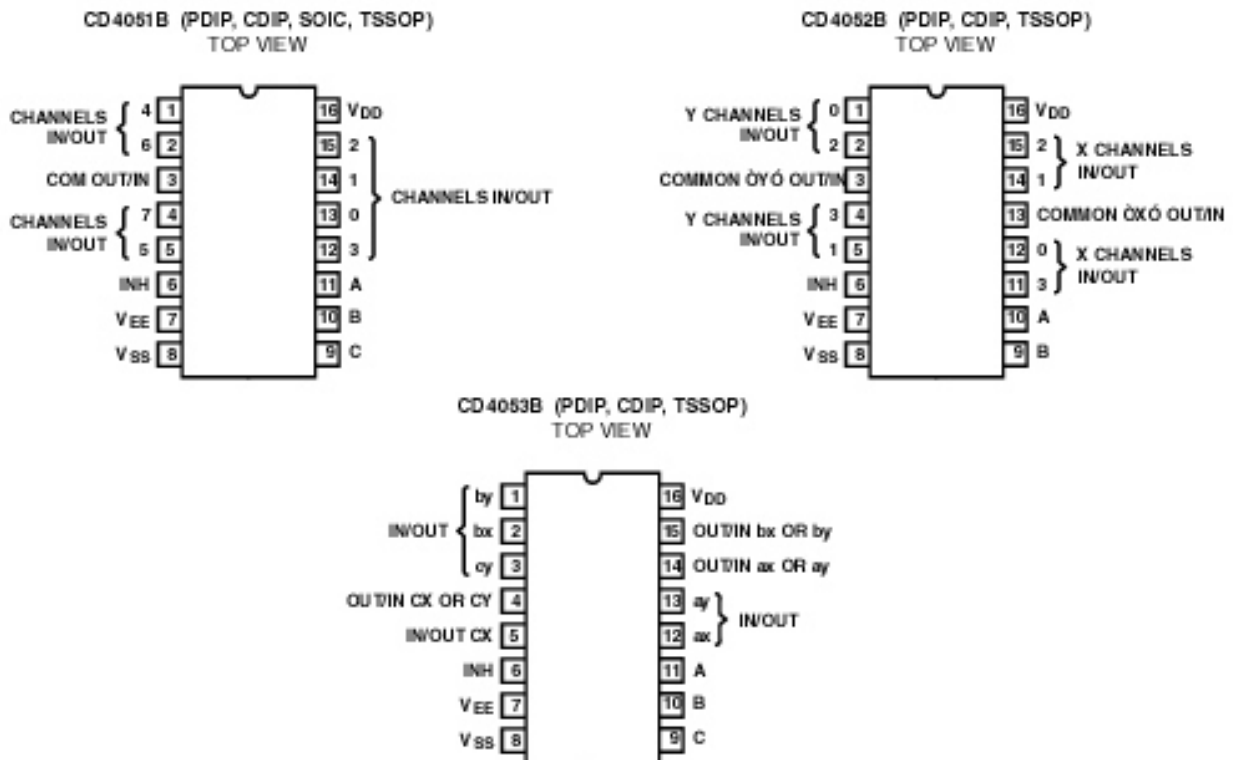
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BNS	-55 to 125	16 Ld SOIC
CD4051BPW, CD4052BPW, CD4053BPW	-55 to 125	16 Ld TSSOP

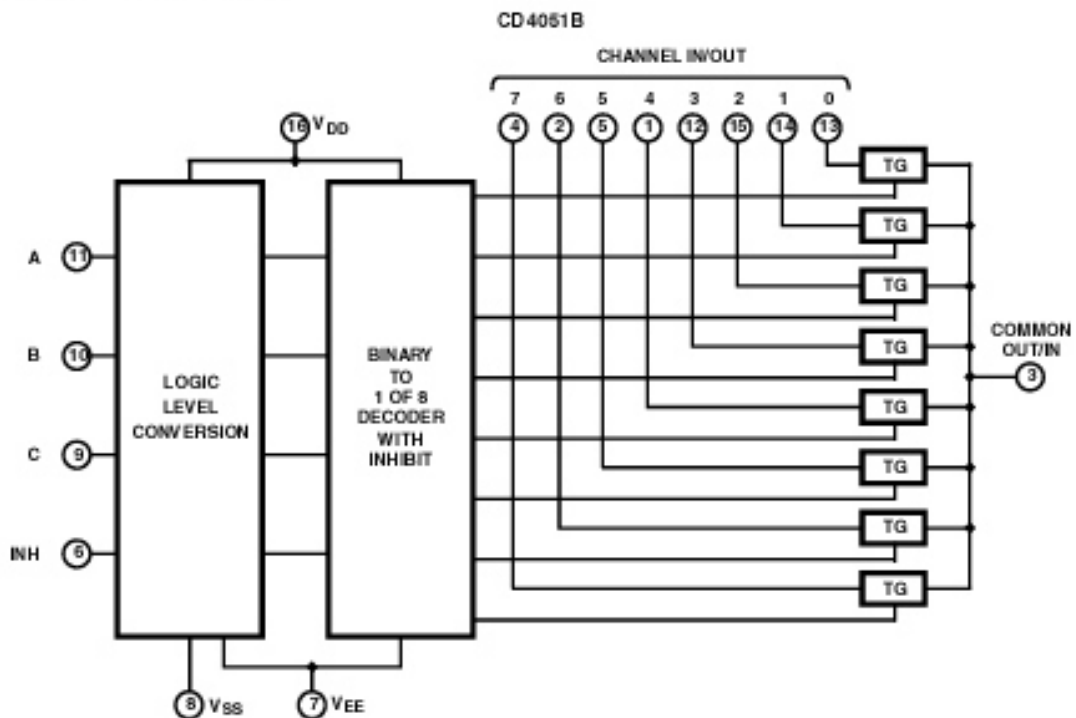
5. INTERNAL BLOCK DIAGRAM OF ICS

CD4053B

Pinouts



Functional Block Diagrams

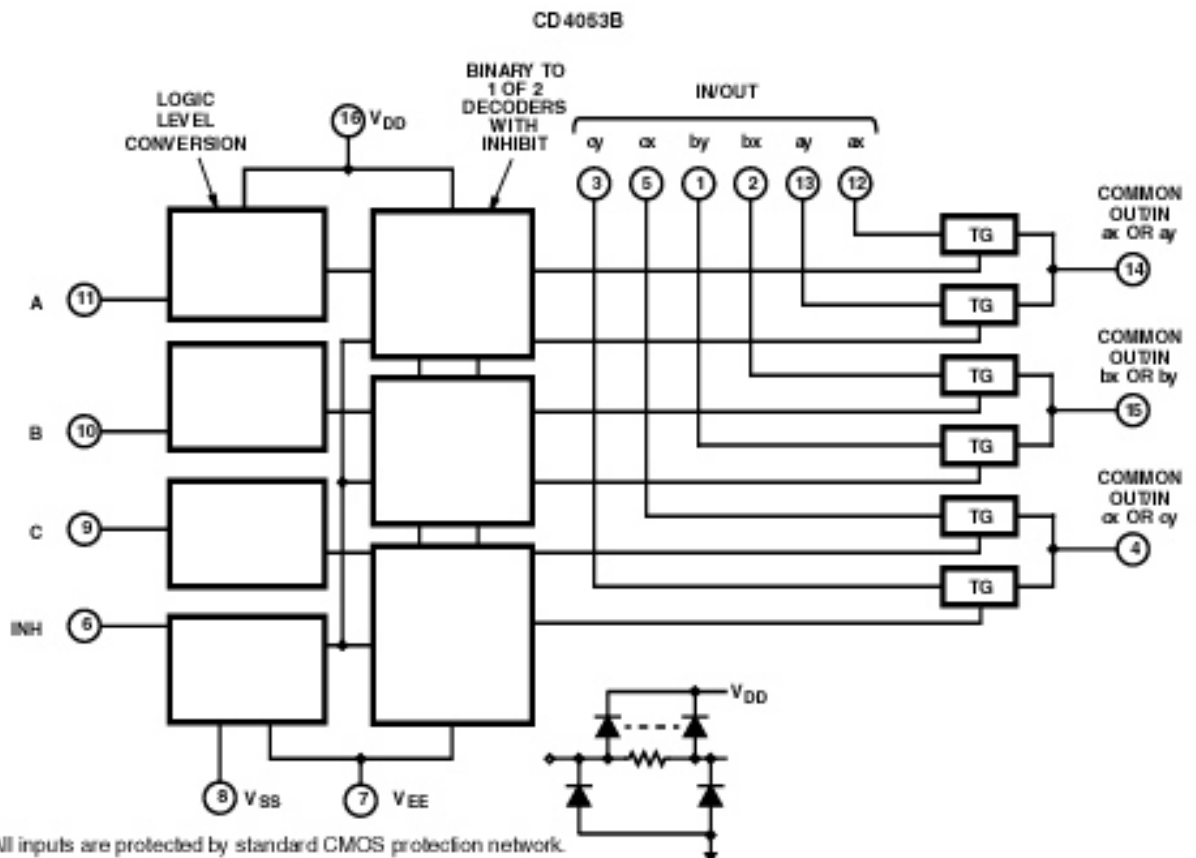
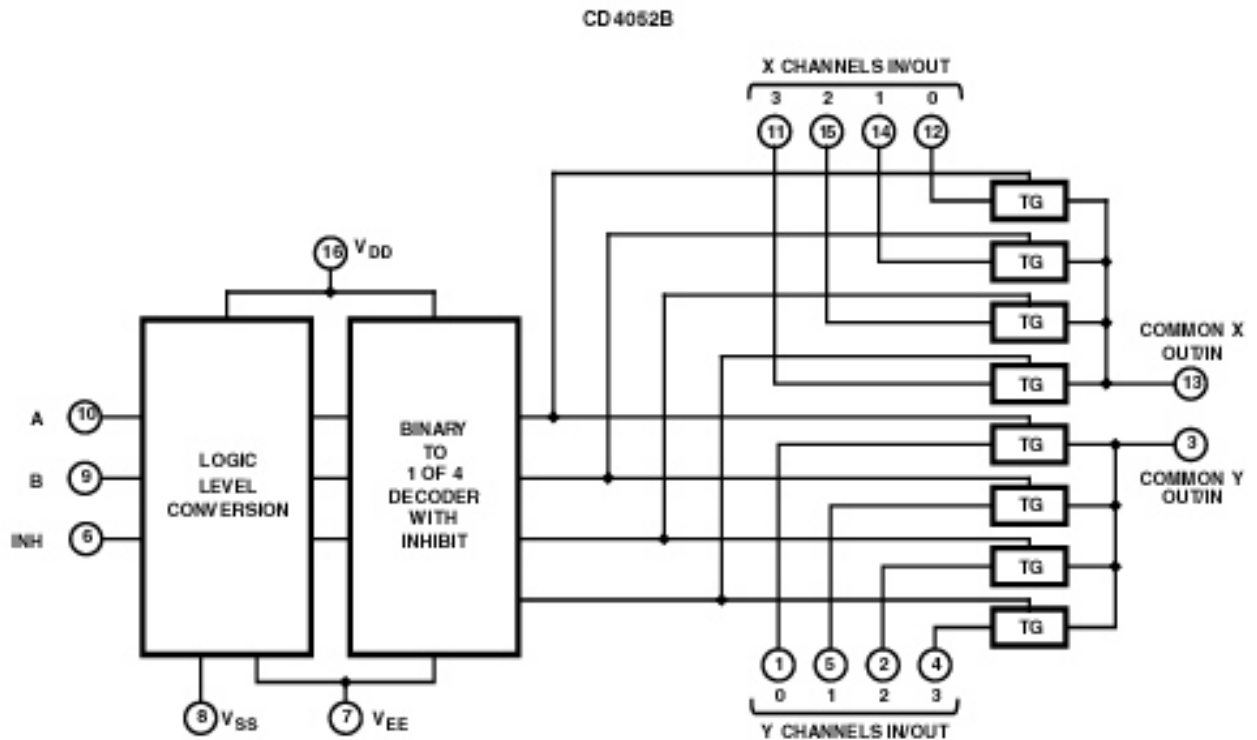


All inputs are protected by standard CMOS protection network.

5. INTERNAL BLOCK DIAGRAM OF ICS

CD4053B

Functional Block Diagrams (Continued)



5. INTERNAL BLOCK DIAGRAM OF ICS

JRC 4558

SLOS073A ± MARCH 1978 ± REVISED JUNE 1999

Continuous-Short-Circuit Protection
Wide Common-Mode and Differential Voltage Ranges
No Frequency Compensation Required
Low Power Consumption
No Latch-Up
Unity-Gain Bandwidth . . . 3 MHz Typ
Gain and Phase Match Between Amplifiers
Low Noise . . . 8 nV/√Hz Typ at 1 kHz
Designed To Be Interchangeable With Raytheon RC4558 and RM4558 Devices

D, JG, P, OR PS PACKAGE
(TOP VIEW)



description

The RC4558 and RM4558 devices are dual general-purpose operational amplifiers with each half electrically similar to the μ A741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RC4558 is characterized for operation from 0°C to 70°C, and the RM4558 is characterized for operation over the full military temperature range of $\pm 55^\circ\text{C}$ to 125°C.

AVAILABLE OPTIONS

T _A	V _{IO} MAX AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE (D)	SSOP (DBR)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SOP (PSR)
0°C to 70°C	6 mV	RC4558D	RC4558DBR	Ø	RC4558P	RC4558PSR
$\pm 55^\circ\text{C}$ to 125°C	6 mV	Ø	Ø	RM4558JG	Ø	Ø

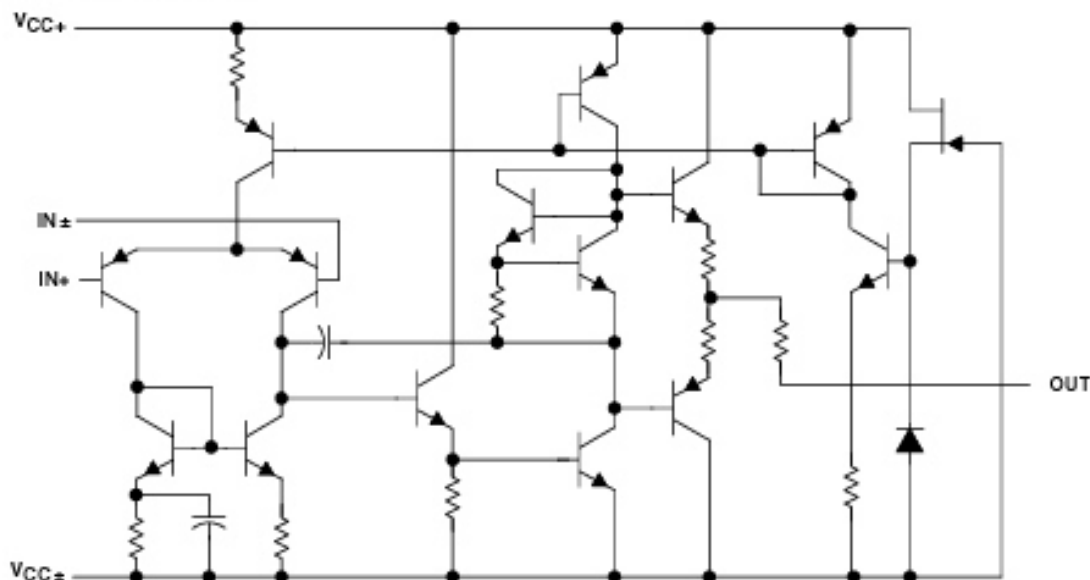
The D package is available taped and reeled. Add the suffix R to the device type (e.g., RC4558DR).

5. INTERNAL BLOCK DIAGRAM OF ICS

JRC 4558

SLOS073A ± MARCH 1976 ± REVISED JUNE 1999

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RC4558	RM4558	UNIT
Supply voltage (see Note 1)	V_{CC+}	18	22	V
	V_{CC-}	±18	±22	
Differential input voltage (see Note 2)		+30	+30	V
Input voltage (any input, see Notes 1 and 3)		+15	+15	V
Duration of output short circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	
Package thermal impedance, θ_{JA} (see Note 5)	D package	197		°C/W
	P package	104		
	PS package	163		
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260		°C
Storage temperature range, T_{stg}		±65 to 150	±65 to 150	°C

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
 5. The package thermal impedance is calculated in accordance with JE5D 51, except for through-hole packages, which use a trace length of zero.

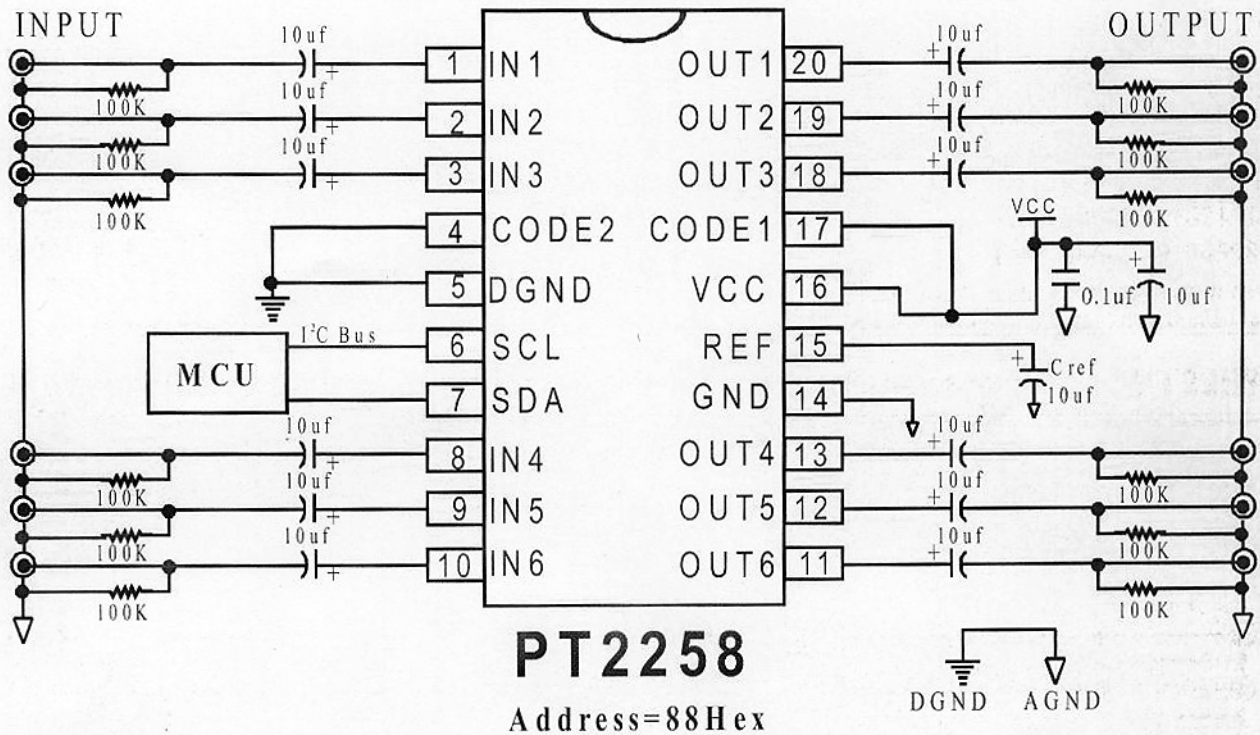
recommended operating conditions

		MIN	MAX	UNIT
Supply voltage	V_{CC+}	5	15	V
	V_{CC-}	±5	±15	
Operating free-air temperature, T_A	RC4558	0	70	°C
	RM4558	±55	125	

5. INTERNAL BLOCK DIAGRAM OF ICS

Pt2558

APPLICATION CIRCUIT



ORDER INFORMATION

Valid Part Number	Package Type
PT2258	20 Pins, DIP Package (300 mil)
PT2258-S	20 Pins, SO Package (300 mil)

5. INTERNAL BLOCK DIAGRAM OF ICS

Pt2558

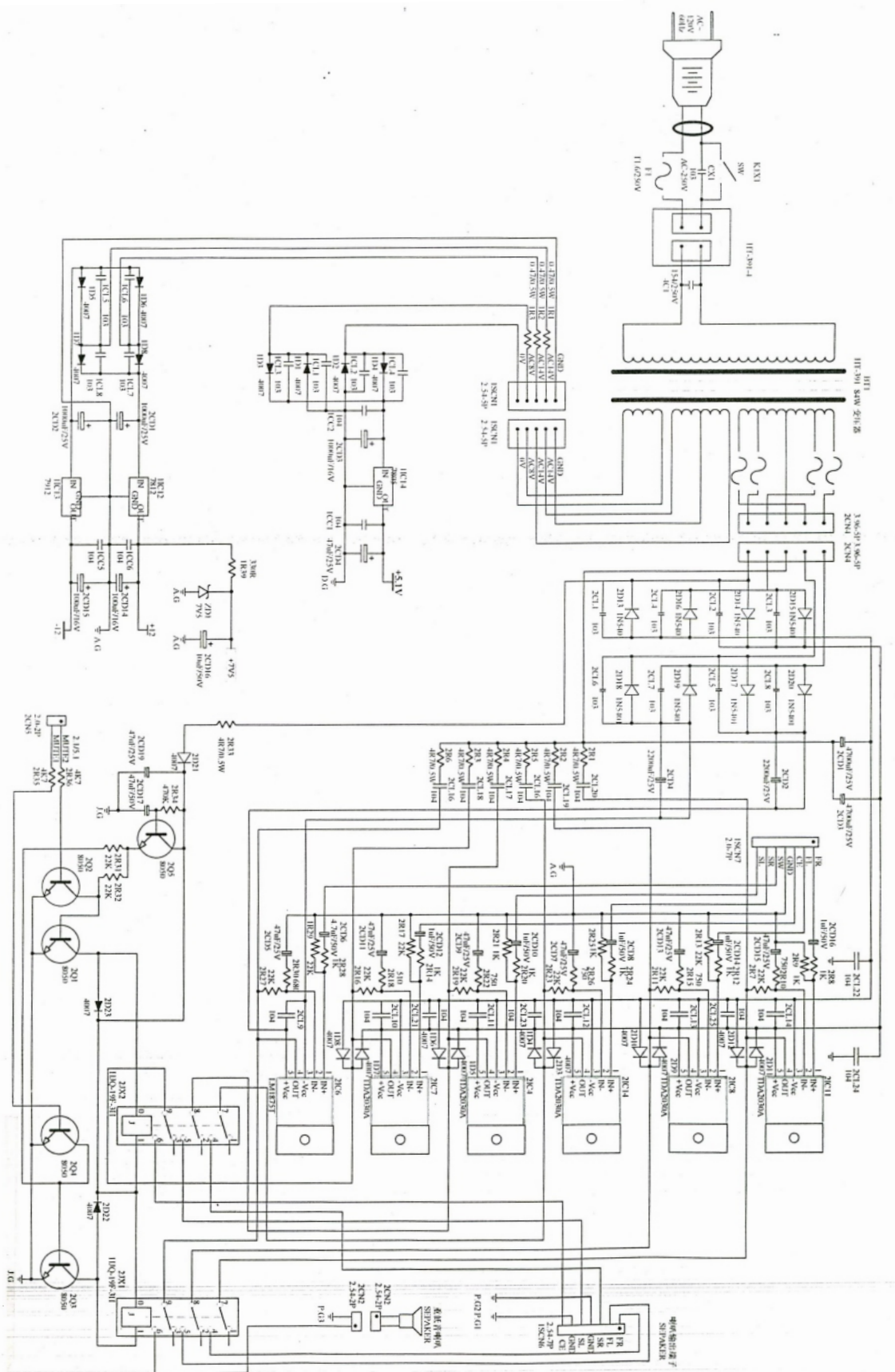
ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply Voltage		5	9	10	V
Is	Supply Current			8		mA
RIN	Input Impedance	FL,FR,CTR SUB,SL,SR	27	30	35	K Ω
VCL	Maximum Input Voltage	Volume=0dB THD=1%		2.8	3.0	Vrms
Sc	Channel Separation		90	100	110	dB
CRANGE	Volume Control Range			79		dB
AVMAX	Maximum Attenuation			-79		dB
Astep	Attenuation Step			1		dB
EA	Attenuation Error	Volume=0~-50dB	-1.0	0	+1.0	dB
AMUTE	Mute Attenuation	A-weighting	90	95	98	dB
THD	Total Harmonic Distortion	Volume=0dB Input,200mVrms	0.003	0.005	0.01	%
Noise	Output Noise	A-weighting		3	5	μ V
S/N	Signal-to-Noise Ratio	0dB=1Vrms A-weighting	100	105	110	dB
Ro	Output Impedance			600	900	Ω
Go	Output Gain		-0.5	0	+0.5	dB
Vomax	Maximum Output	FL,FR,CENTER SUB,SL,SR THD=1%	2.3	2.6	2.9	Vrms

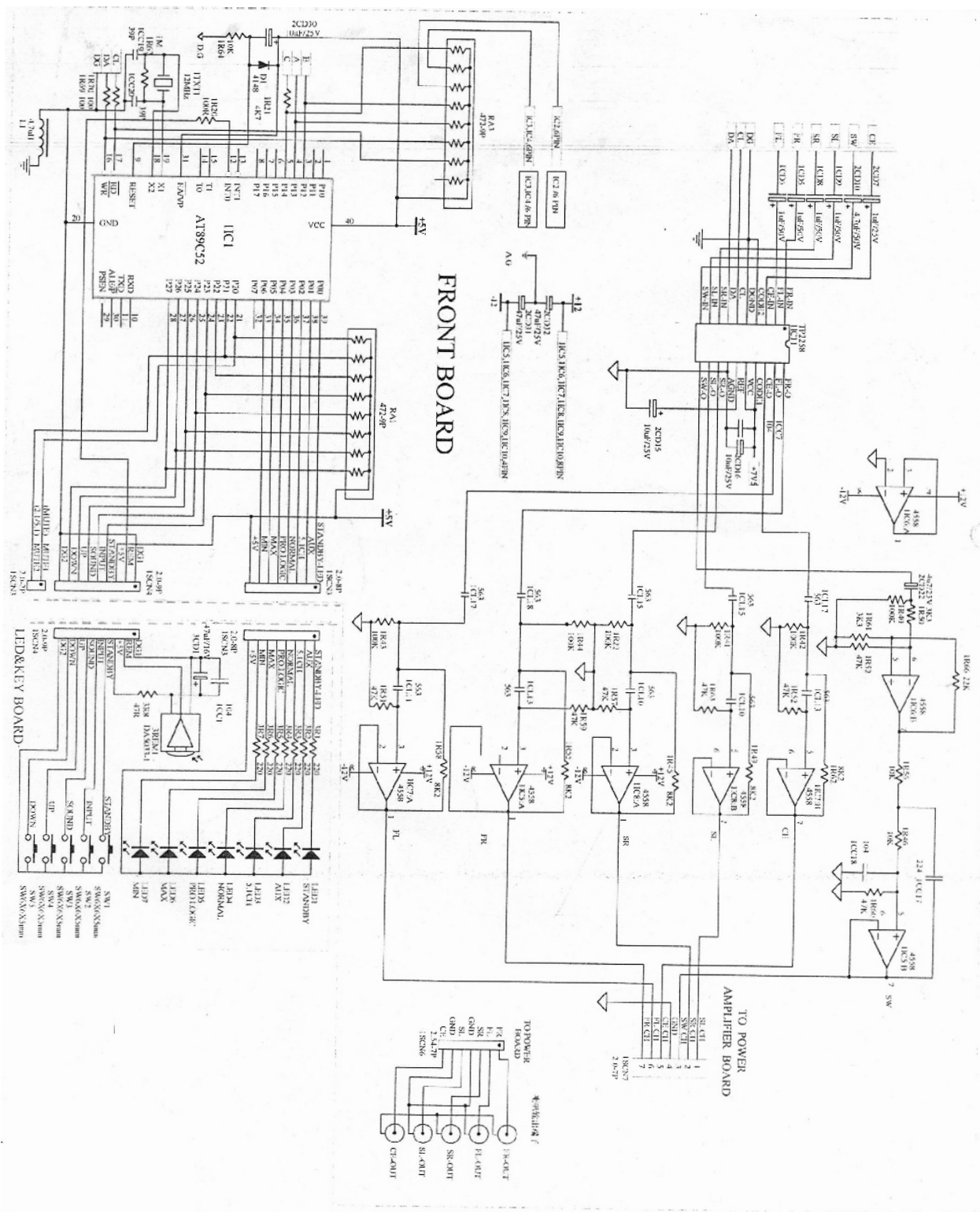
I²C BUS SECTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIL	Bus Low Input Level			2.4	2.5	V
VIH	Bus High Input Level		2.8	3.0		V
TINIT	Bus Initialization	Cref=10 μ F		250	300	mS

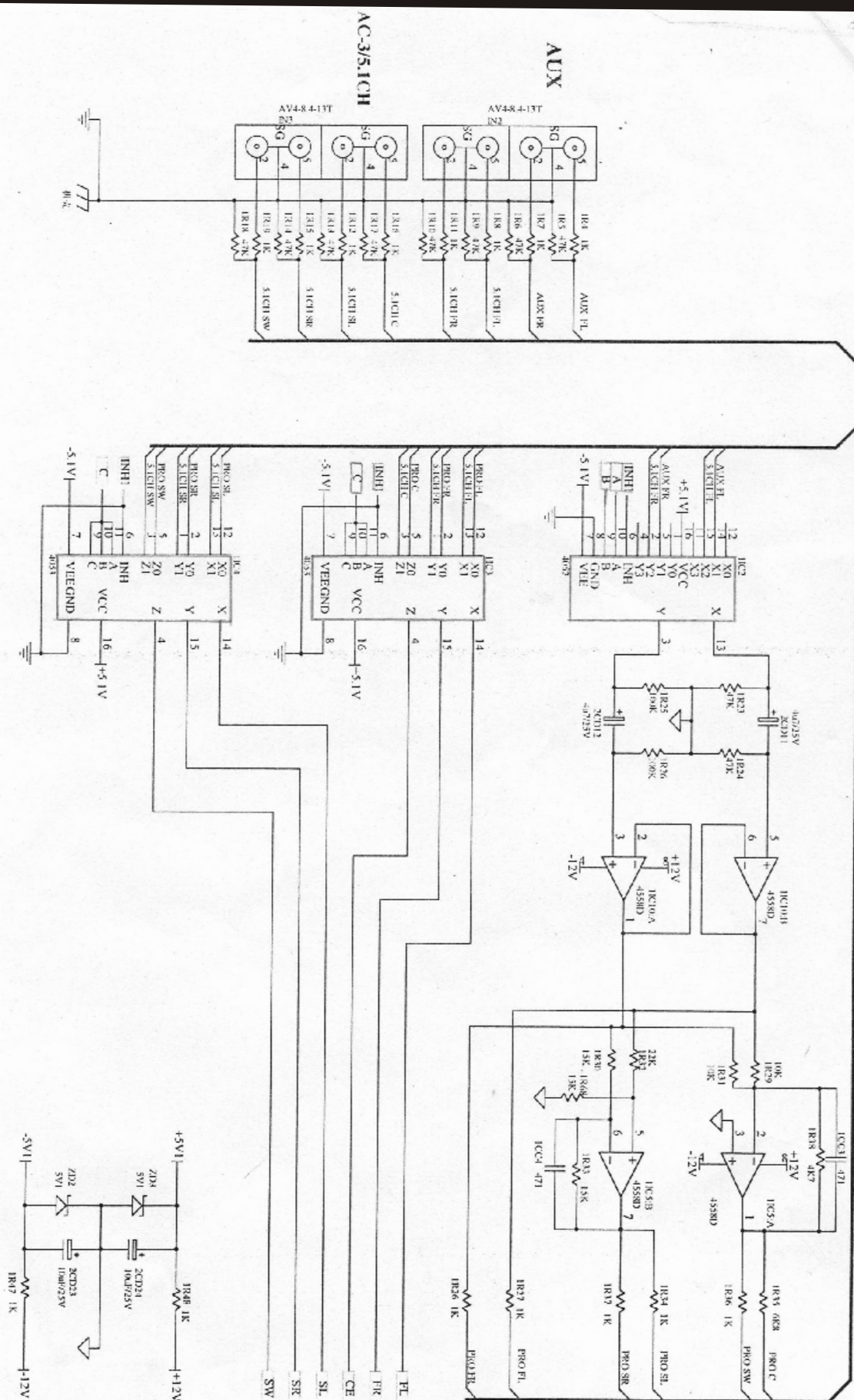
6. SCHEMATIC DIAGRAM



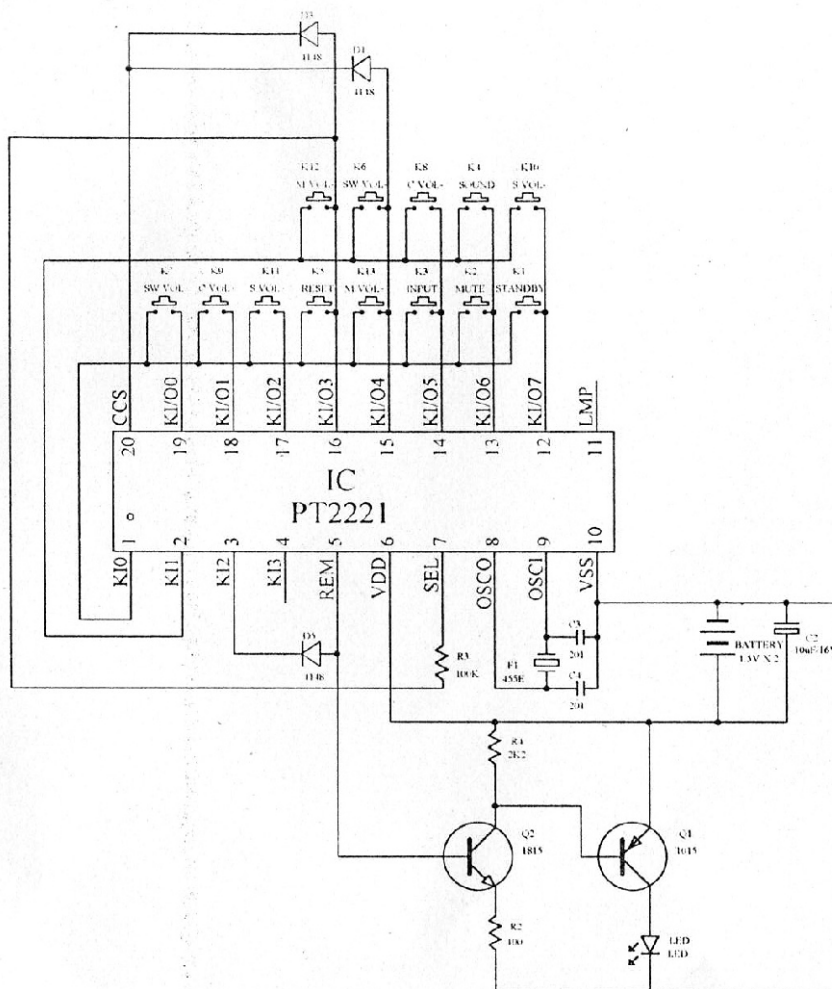
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REMOTE CONTROL BOARD